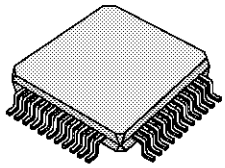
SGS-THOMSON MICROELECTRONICS

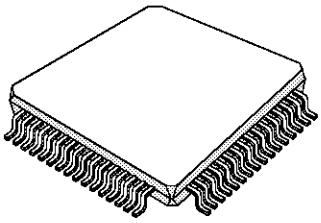
ST75C502

V.32bis/V.17 HIGH SPEED MODEM DATA PUMP

- 2 CHIP DATA PUMP (ST75C502, ST7544)
- V.32BIS, V.17, V.33, V.32, V.29, V.27ter, V.22BIS, V.22, V.21, V.23, BELL212A, 103 (SHORT TRAIN INCLUDING V.29/T104)
- GROUP 3 FAX AT 14400, 12000, 9600, 7200, 4800, 2400BPS
- PARALLEL/SERIAL SYNCHRONOUS DATA HANDLING
- DIGITAL FAR AND NEAR END ECHO CANCELLATION SUPPORTING A DELAY OF 2 SATELLITE HOPS (1.6 seconds) AND PHASE ROLL UP TO 10Hz
- AUTODIAL AND AUTOANSWER
- COMPLETE HANDSHAKE MANAGEMENT
- WIDE DYNAMIC RANGE (> 48dB)
- COMPROMISE TRANSMIT EQUALIZER
- AUTOMATIC ADAPTIVE EQUALIZER
- VOICE MODE (A LAW)
- ENHANCED PROGRAMMABLE TONE DETECTOR (INCLUDING DTMF)
- AUTO MODE (WITH MCU SUPPORT)
- ITU-T V.54 SIGNALLING
- ANCILLARY CONVERTERS FOR EYE PATTERN MONITORING
- VERSATILE INTERFACES
  - PARALLEL 64x8 DUAL PORT RAM
  - SYNCHRONOUS SERIAL I/O
  - AUXILLIARY PARALLEL I/O
- CALLER ID DEMODULATION
- LOW PROFILE TQFP PACKAGE OPTION



TQFP44
(Plastic Quad Flat Pack)



TQFP80
(Plastic Quad Flat Pack)

ORDERING INFORMATION

Sales Type	Function	Package
ST7544 CQFP	Mafe	TQFP 44
ST7544 CFN	Mafe	PLCC 44
ST75C502 CQFP	Romed DSP	TQFP 80
ST18933 PQFP	Customisable DSP	PQFP 160
STI8933 EMU-PC	PC Software Developement Tool	PC BOARD
SATURN	Modem Application with Protocols (V.42bis/FAX)	BOARD/CS

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I - GENERAL DESCRIPTION

This highly integrated modem consists of 2 chips, the first being a dedicated DSP (ST75C502), the second being the ST7544 MAFE. Emphasis has been put on performance and size/power consumption for portable applications.

This product gives a high performance modem conformant to ITU-T recommendations V.32bis, V.17, V.33, V.32, V.29, V.27ter, V.22bis, V.22, V.21 and V.23. Also Bell 212A and 103.

As a data modem the ST75C502 can operate at 14400, 12000, 9600, 7200, 4800, 2400, 1200, 300 or 75 bits per second as standard. As a fax, the ST75C502 fully supports group 3 send and receive speeds of 14400, 12000, 9600, 7200, 4800 and 2400 bits per second.

Programmable features allow the product to be tailored to a wide range of high speed modem requirements.In addition, to add to the flexibility of this product, the customer can develop, on a similar hardware platform to the standard product, proprietary code for ROMing into the memory of the DSP. If required, ability to access external memory of up to 64K x 32 is given such that customer specific modes of operation can be added and easily updated.Code development is made simple via a slot in PC development card and is fully supported by SGS-THOMSON (STI8933 PC-EMU).

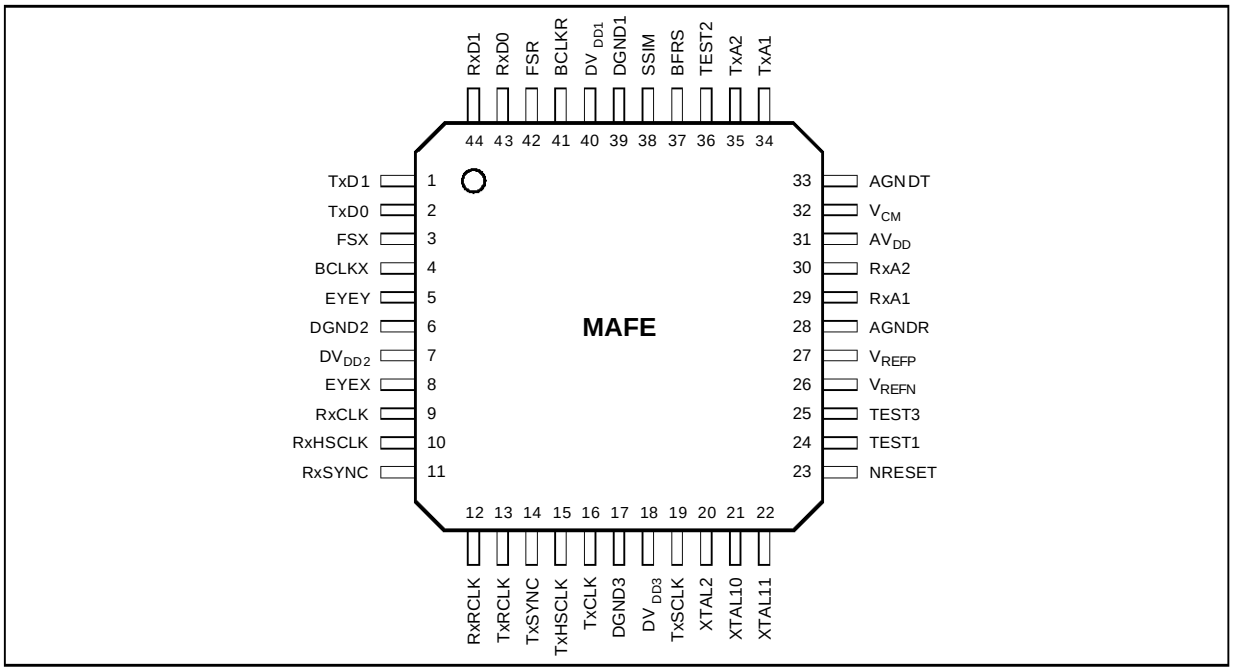
The voice mode allows for implementation of enhanced telephony functions such as answering machines.

For customer specific code requiring access to external memory, a 160 pin flatpack containing the DSP and a 44 pin flatpack containing the MAFE are also available (type numbers ST18933 and ST7544 respectively).

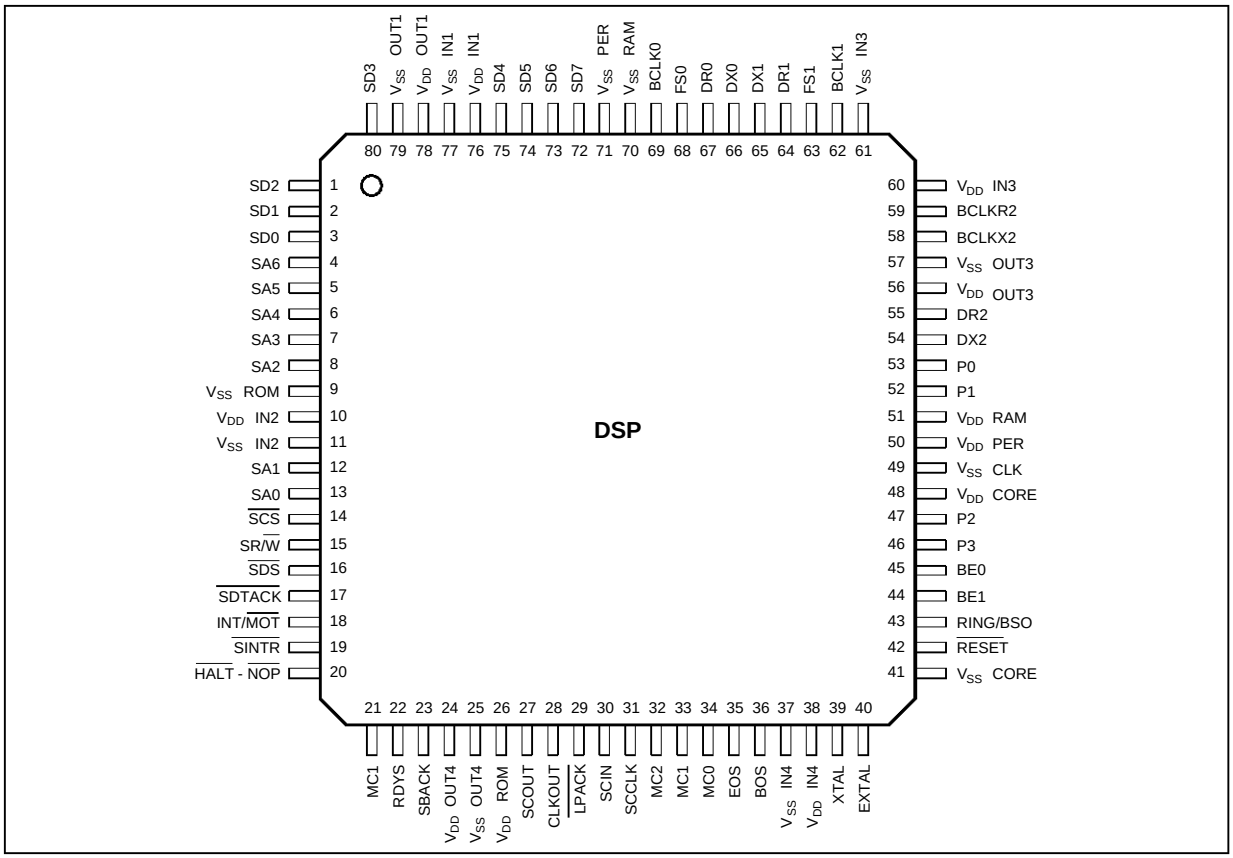
Further information on the DSP (STI8933) and MAFE (ST7544) can be found in the relevant datasheets

II - PIN CONNECTIONS

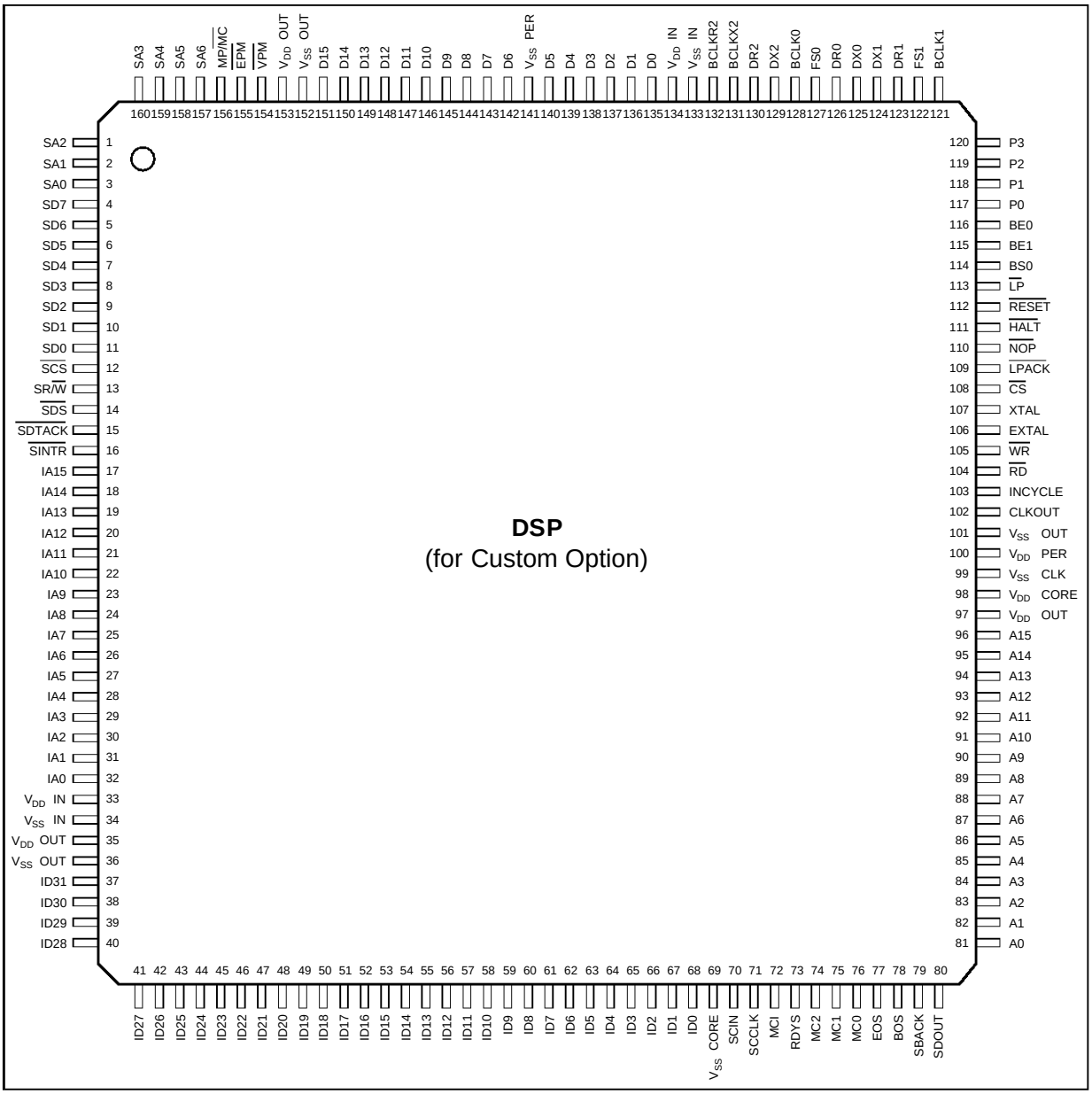
II.1 - ST7544CQFP Top View (TQFP44)



II.2 - ST75C502CQFP Top View (TQFP80)



II.3 - ST18933PQFP Top View (PQFP160)



III - PIN DESCRIPTION

See Figure F2 in appendix F for complete schematics.

III.1 - Host Interface

The exchanges with the control processor proceed through a 64 Bytes DUAL port RAM shared between the DSP and the Host. The pins associated with this interface are :

Pin Name	Type	Description
SD0..SD7	I/O	System Data Bus. 8-bit data bus used for asynchronous exchanges between the ST75C502 and the Host through the DUAL port RAM. High impedance when exchanges are not active.
SA0..SA6	I	System Address Bus. 7-bit address bus for DUAL port RAM.
$\overline{\text{SDS}}$ ($\overline{\text{SDS}}$)	I	System Data Strobe. Active low. Synchronizes all the exchanges. In Motorola mode initiates the exchange, active low. In Intel mode initiates a read exchange, active low.
SR/$\overline{\text{W}}$ ($\overline{\text{SWR}}$)	I	System Read/Write. In Motorola mode defines the type of exchange read/write. In Intel mode initiates a write exchange, active low.
$\overline{\text{SCS}}$	I	System Chip Select. Active low.
$\overline{\text{SDTACK}}$	O	System Bus Data Acknowledge. Active low.
$\overline{\text{SINTR}}$	O	System Interrupt Request. Active low. This signal is asserted by the ST75C502 and negated by the Host.
$\overline{\text{RESET}}$	I	Reset. Active low.
$\overline{\text{RING}}$	I	Ring Detect Signal. Active low.
INT/$\overline{\text{MOT}}$	I	Select Intel/Motorola Interface.

III.2 - Serial Interface

The transmit and receive synchronous data exchanges between the DSP and microprocessor can pass via the Simplified Synchronous Serial Interface. Two pins are allowed for the data :

Pin Name	Type	Description
DR2	O	Synchronous Data Output
DX2	I	Synchronous Data Input

III.3 - Auxiliary Interface

A set of auxiliary signals are provided to simplify the DAA Interface. This is made by a three line General Purpose Parallel Input/Output.

Pin Name	Type	Description
PO	I/O	Parallel Input/Output 0
P1	I/O	Parallel Input/Output 1
P2	I/O	Parallel Input/Output 2

III.4 - Miscellaneous

Pin Name	Type	Description
XTAL	O	Internal oscillator Output. Left open if not used.
EXTAL	I	Internal oscillator Input, or External Clock
CLKOUT	0	Internal clock (XTAL frequency divided by 2)

Note : The nominal external clock frequency of the DSP is 36.864MHz. The nominal external clock frequency of the MAFE is 18.432MHz with a precision better than $\pm 5.10^{-5}$ (and is output from the DSP on the CLKOUT Pin).
When in Sleep Mode the CLKOUT clock is not available.

III.5 - Mafe Interface

A set of signals is use for interconnection between the DSP and the Analog Front End.

Pin Name		Description
DSP	MAFE	
P3	NRESET	Reset of the Analog Front End
BCLK0	BCLKR	Receive Serial I/O Clock
FS0	FSR	Receive Serial I/O Frame Synchro
DX0	RXDI	Receive Serial I/O Input
DR0	RXDO	Receive Serial I/O Output
BCLK1	BCLKX	Transmit Serial I/O Clock
FS1	FSX	Transmit Serial I/O Frame Synchro
DX1	TXDI	Transmit Serial I/O Input
DR1	TXDO	Transmit Serial I/O Output
BCLKX2	RXCLK	Receive Bit Clock
BCLKR2	TXCLK	Transmit Bit Clock
BE0	RXRCLK	Receive Baud Clock
BE1	TXRCLK	Transmit Baud Clock

III.6 - Power Supply

Pin Name	Number	Description
V_{DD}	11	+5V Supply (Pins 10, 24, 26, 38, 48, 50, 51, 56, 60, 76, 78)
V_{SS}	12	0V (Pins 9, 11, 25, 37, 41, 49, 57, 61, 70, 71, 77, 79)

III.7 - Boundary Scan Interface

A set of 13 signals are dedicated for Testing the DSP. These signals can be used in a development phase, associated with SGS-THOMSON ST18932 Boundary Scan Development Tools, to Debug the application Hardware and Software. Input signals must be grounded.

Pin Name	Type	Description
SCIN	I	Scan Data Input
SCCLK	I	Scan Clock
SCOUT	O	Scan Data Output
BOS	I	Begin of Scan Control
EOS	I	End of Scan
MC0..MC2	I	Mode Control
SBACK	O	Software Breakpoint Acknowledge
MCI	O	Multicycle Instruction
RDYS	O	Ready to Scan Flag
$\overline{\text{HALT}}$	I	Stop ST75C502 Execution. Active Low.
$\overline{\text{LPACK}}$	O	Acknowledge Low Power Mode

IV. - ELECTRICAL SPECIFICATIONS

Unless otherwise specified, electrical characteristics are specified over the operating range. Typical value are given for V_{DD} = +5V and T_{amb} = 25°C and for nominal crystal frequency of 36.864 MHz.

IV.1 - Maximum Ratings (referenced to GND)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.3, +7.0	V
V_I, V_{IN}	Digital Input Voltage	-0.3, V_{DD} + 0.3	V
I_I, I_{IN}	Digital Input Current	± 1	mA
I_O	Digital Output Current	± 20	mA
T_A	Operating Temperature	0, +70	°C
T_{stg}	Storage Temperature (plastic)	-40, +125	°C
P_{tot}	Maximum Power Dissipation	TBD	mW

Stresses above those hereby listed may cause damage to the device. The ratings are stress related only and functional operation of the device in conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

IV.2 - DC Characteristics

V_{DD} = 5V ± 5%, GND = 0V, T_A = 0 to 70°C (Unless otherwise specified).

IV.2.1 POWER SUPPLY AND COMMON MODE VOLTAGE

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.75	5	5.25	V
I_{DD}	Supply Current		110		mA
I_{DD}-LP	Supply Current in Low Power Mode		8		mA

IV.2.2 - Digital Interface

All digital pins except XTAL pins.

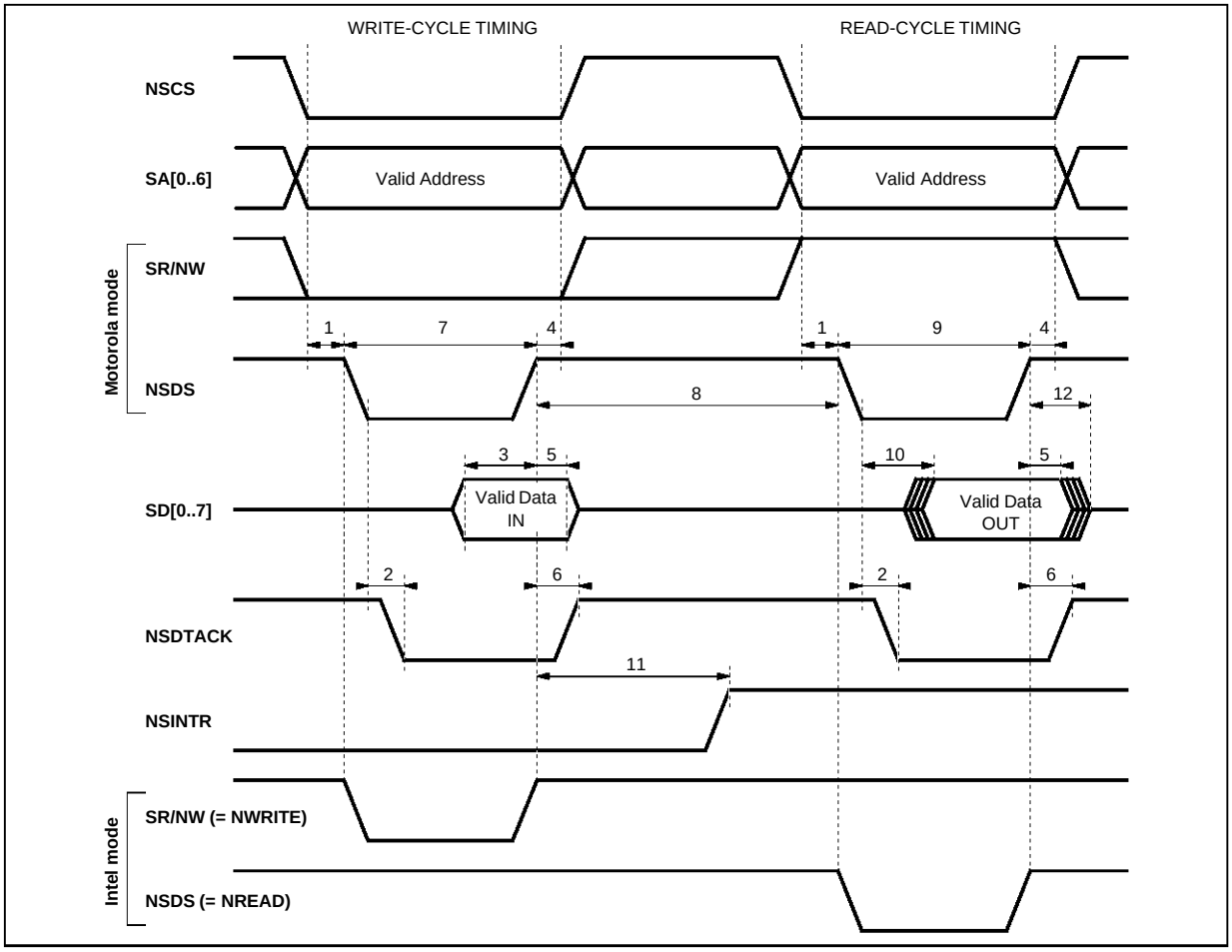
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage	-0.3		0.8	V
V_{IH}	High Level Input Voltage	2.4			V
I_I	Input Current V_I = V_{DD} or V_I = GND	-10	0	+10	µA
V_{OH}	High Level Output Voltage (I_{LOAD} = 2mA)	2.8			V
V_{OL}	Low Level Output Voltage (I_{LOAD} = 2mA)			0.5	V
I_{OZ}	Three State Input Leakage Current (GND < V_O < V_{DD})	-10	0	10	µA
C_{IN}	Input Capacitance		5		pF

IV.2.3 - Crystal Oscillator Interface (XTAL, EXTAL)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage			0.8	V
V_{IH}	High Level Input Voltage	2.7			V
I_L	Low Level Input Current GND < V_I < V_{ILmax}	-20		-7	µA
I_H	High Level Input Current V_{IHmin} < V_I < V_{DD}	7		20	µA

IV.3 - AC Electrical Characteristics
IV.3.1 - Dual Port Ram Host Timing

Figure 1

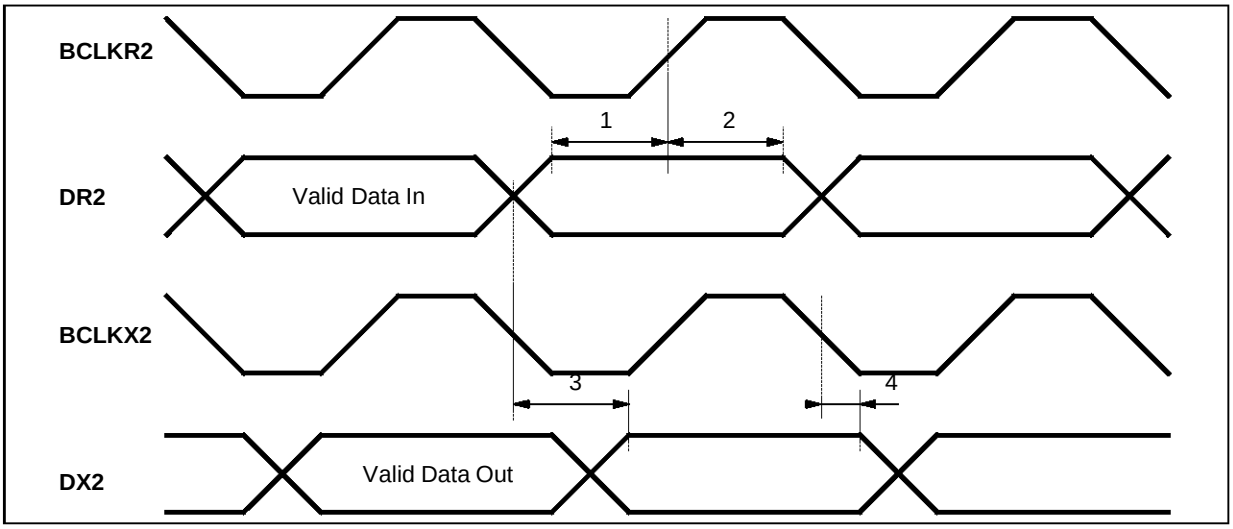


Number	Description	Min.	Typ.	Max.	Unit
1	Address and Control Setup Time	5			ns
2	SDTACK Acknowledge			20	ns
3	Data Setup Time	10			ns
4	Address and Control Hold Time	0			ns
5	Data Hold Time	5			ns
6	SDTACK Hold Time	0			ns
7	Write Enable Low State	45			ns
8	Access Inhibition High State (1)	70			ns
9	Read Enable Low State	45			ns
10	Read Data Access			35	ns
11	SINTR Clear Delay			50	ns
12	Data Valid to Tristate			15	ns

Note 1 : A minimum delay of 70ns is required only from the rizing edge of NWRITE to the falling edge of the next selected NREAD or NWRITE.

IV.3.2 - Serial Interface Timing

Figure 2



Number	Description	Min.	Typ.	Max.	Unit
1	DR2 to BCLKR2 Set-up Time	30			ns
2	DR2 to BCLKR2 Hold Time	10			ns
3	DX2 Valid to BCLKX2 Delay Time			100	ns
4	DX2 to BCLKX2 Hold Time. DX2 Signal is High Z Just After Reset	0			ns

V - FUNCTIONAL DESCRIPTION

V.1 - System Architecture

The system is based on a two-chip set. The first chip is the ST75C502 dedicated DSP handling all the signal processing routines for transmission, reception and echo cancellation on modem signals. It also holds the tone generators and detectors. Alternately the ST18933 DSP is available for customer specific operations. The second chip is the ST7544 delta-sigma MAFE, which performs the AD/DA conversions as well as the signal pre or post-filtering, and the sampling interpolation on the echo cancellation path.

The chip set allows the design of a complete V.32bis data-pump without any external component. A versatile dual port RAM allows an easy interface with most popular micro-controllers.

V.2 - Chip Set Interconnect Circuitry

Please refer to appendix F for a detailed schematic of the chip set interconnect circuitry.

V.3 - Operation

V.3.1 - Modes

The modem implementation is fully compatible with many popular ITU-T and Bell recommendations. The modulation can be either Trellis Coded Modulation (TCM) as in V.33 14400, 12000, V.32bis 14400, 12000, 9600, 7200, V.32 9600 bps rates, Quadrature Amplitude Modulation (QAM) as in V.32bis 4800, V.32 9600, 4800, V.22bis 2400, Differential Phase Shift Keying (DPSK) as in V.22 1200, Bell 212A 1200 bps rates, or Frequency Shift Keying (FSK) as in V.21, V.23 and Bell 103 modes. Both the bit rate and the treillis options are determined during the initial modem handshake sequence. V.29, V.27ter and V.17 are also available for FAX transmission. Other modes of operation include tone and DTMF detection or generation and voice mode.

V.3.2 - Transmitter Description

The signal pulses are shaped in a dedicated filter combined with a compromise transmit equalizer suited for transmission over strongly distorted lines. 2 different compromise equalizers are available and can be selected by software. User defined transmit equalizers can be downloaded in the DSP RAM.

V.3.3 - Echo Canceller Description

The echo canceller consists of a near end and a far end echo canceller. Both are fractionally spaced and achieve a high cancellation of the echo paths. The receive signal reconstruction is purely digital by virtue of the MAFE architecture. The far end echo requires either an external low cost 8kx8-100ns memory (for the customisable product STI8933), or the allocation of an equivalent amount of RAM in the controller memory space. It also sustains up to 10Hz of frequency offset on the far end echo path without degradation of performance.

V.3.4 - Receiver Description

The receiver section handles complex signals and uses a fractionally spaced complex equalizer. It is able to cope with distant modem frequency drifts up to 10^{-4} as specified in the ITU-T recommendations. It also compensates for phase jitter at multiple and simultaneous frequencies.

V.3.5 - Tone Generator Description

Four tones can be simultaneously generated by the ST75C502. The tones are determined by their frequencies and by the output amplitude level. A set of specific command is also available for DTMF generation (using two of the four generators available).

V.3.6 - Tone Detector Description

16 tones can be simultaneously detected by the ST75C502. Each of the tones to be detected is defined by the coefficients of a 4th order programmable IIR. Detection thresholds are also programmable from -45dBm up to -10dBm.

V.3.7 - DTMF Detector Description

A DTMF detector is included In the ST75C502, it permits detection of valid DTMF digits. A valid DTMF digit is defined as a dual tone with total power higher than -35dBm, duration greater than 40ms and differential amplitude within 8dB (positive or negative).

V.3.8 - Voice Mode Description

The ST75C502 voice mode allows the implementation of enhanced telephony functions such as answering machines. Incoming samples (7200Hz) from the line are PCM-A-law coded and are written into the dual port RAM. The outgoing samples are decompressed using the same A-law and are output to the telephone line.

The voice mode is entered using a CONF command, it can be either transmit voice from the dual RAM Tx buffer to the telephone line, receive voice from the telephone line to the dual RAM buffer, or both of these functions simultaneously. The format of the signal is A-law coded without complementation of the even bits. The buffer mechanism, between the host micro-controler and the ST75C502 is identical to the mechanism used for parallel data exchanges except that it starts immediately after CONF command, the size of the transmit and received buffer, are and must be 8 bytes, there is no need for a XMIT command, and if an overrun or underrun condition occurs no error will be reported to the host processor.

V.3.9 - Analog Loop Back Test Mode

In any transmission standard and any data format, the ST75C502 can be configured for analog loop back test

V.3.10 - Digital Loop Back Test Mode

These loop back modes comply with the test loop 2 of the ITU-T V.54 recommendation for V.32 and V.32 bis. For V.22 and V.22 bis the digital loop back modes comply with these recommendations.

V.3.11 - Low Power Mode

When entering the low power mode all the peripherals of the DSP core are stopped in order to reduce the power consumption, the ST7544 is set in low power mode. The dual RAM is made inaccessible.

A hardware RESET must awake the ST75C502.

V.3.12 - Reset

After a hardware RESET, or an INIT command, the ST75C502 clears all its internal memories, clears the whole DUAL RAM and starts to initialize the ST7544 Delta Sigma Analog converters. As soon as these initializations are completed, the ST75C502 clears the DUAL RAM address 0 (COMSYS), generates an interrupt IT6 (command Acknoledge) and is programmed to send and receive tones, the bit clocks are programmed to 9600Hz. The transmit sample clock is set to 7200Hz and the receive sample clock to 9600Hz.

The total duration of this "cold" RESET sequence is about 500ms. After that time the ST75C502 is ready to execute commands sent by the host micro-controler. Be carrefull that any command send in this reset time will be lost.

The minimum duration of the RESET signal is 700ns.

In order to speed up the RESET time, a "Warm" initialization is possible using the INIT 01 command ; in this case the RESET time is less than 10ms ; the only difference is that the ST7544 is not initialized again.

V.4 - Modem Interface

V.4.1 - Analog Interface

The modem designer must provide a proper hybrid interface to the ST7544. An example of hybrid design is given in appendix F (see Figure F1). The inputs and outputs of the MAFE are differential, thus achieving better noise immunity.

V.4.2 - Host Interface

The host interface is seen by the micro as a 64x8 RAM, with additional registers accessible through an 7-bit address space. This RAM can be used for data transmission using the SERIAL command.

V.4.3 - Auxiliary Parallel Interface

The auxiliary parallel interface is a general purpose 3-bit parallel interface, which carries various signals, used by the controller and the analog part of the modem. Each pin can be independently programmed for input or output.

V.4.4 - Auxiliary Serial Interface

The auxilliary serial interface is a serial synchronous I/O, which carries the bit data flow.

V.4.5 - Eye Pattern Converters

The output from these two D to A converters on ST7544 provides direct display of the constellation.

VI - USER INTERFACE
VI.1 - Dual Port Ram Description

The dual port RAM is the standard interface between the controller and the ST75C502, for either commands or data. This memory is addressed through a 7-bit address bus. The locations from $00 to $3F are RAM locations, while locations from $40 to $50 are control registers dedicated to the interrupt handling.

Several functional area are defined in the dual port RAM, namely :

- the command area,
- the report area,
- the status area,
- the bulk delay exchange area,
- the data buffer areas.

VI.1.1 - Mapping
VI.1.1.1 - Command Area

The command area is located from $00 to $04. Address $00 holds the command byte COMSYS, and the four next locations hold the parameters COMPAR[0..3]. The command parameters must be entered before the command word is issued. Once the command has been entered, the command byte is reset and an acknowledge report is issued. A new command should not be issued before the acknowledge counter COMACK is incremented. The command exchange rate has a maximum of 2400Hz.

VI.1.1.2 - Report Area

The report area is located from address $05 to address $07. Location $05 holds the acknowledge counter COMACK. Each time a command is acknowledged, the report bytes COMREP[0..1] (if any) are written into locations $06 and $07, and the content of COMACK is incremented. This counter allows an acurate monitoring of the command processing by the ST75C502.

VI.1.1.3 - Status Area

The status area is located from address $08 to $0A. The error status word SYSERR is located at address $08. This error status word is updated each time an error condition occurs. An optional interruption IT0 may be triggered as well in the case of an error condition. Locations $09 and $0A hold the general status bytes STATUS[0..1]. The meaning of the bits depends of the mode of operation, and is described in Appendix B. The third byte at address $0B holds the Quality Monitor byte STAQUA.

VI.1.1.4 - Optional Status Area

The user can program (through the DOSR command) the three locations STAOPT[0..2] of the Optional Status Area ($0C to $0E) for the real time monitoring of three arbitrary memory locations.

VI.1.1.5 - Bulk Delay Exchange Area

This area is reserved for V.32 / V.32bis storage of Far End echo canceller symbols. Refer to Appendix H and application note.

This area has two sub-sections :a flagging section ($0F to $13) and a bulk data area ($14 to $1B).

Location $0F holds the bulk data buffer status SYMSTA. Locations $10 and $11 (resp. $12 and $13) contain a pointer to the bulk data buffer SYMADR[0..1] (resp. SYMADT[0..1]), in the controller space, which should receive (resp. send) the next group of 8 delayed symbols. The ST75C502 manages thus an area of 4k bytes in a circular addressing mode inside the controller memory space. The buffer SYMBUF[0..7] containing the symbols received or sent to the controller is located from $14 to $1B.

VI.1.1.6 - Data Buffer Area

The Data Buffer Area is made of two double 8-byte Buffers. Each of the four buffers is attached to a status byte. This status byte contains the number of valid Data Byte inside the Data Buffer. Within each buffer, D0 represents the first bit in time.

VI.1.2 - Interruptions

The ST75C502 can generate 6 interrupts for the controller. The interrupt handling is made with a set of registers located from $40 to $50.

The interruptions generated by the ST75C502 come from seven different sources. Once the ST75C502 rises an interrupt, a signal is sent to the controller. The controller has then to process the interrupt and clear it. The interrupt source can be examined in the Interrupt Source Register ITSCRC located at $50. According to this status byte, the interrupt source can be determined. Then, writing a zero at one of the memory location $40 to $46 (Reset Interrupt Registers ITREST[0..6]) will reset the corresponding interrupt (and thus acknowledge it). These six sources of interruptions can be masked globally or individually using the Interrupt Mask Register ITMASK located at $4F.

The 7 series interrupt sources are :

IT0 Error/Warning : an error has occurred and the error code is available in the error status byte SYSERR. This byte can be selectively cleared by the CSE command.

IT1 Bulk Delay : the bulk delay buffer requires an action from the controller, for emptying it and for filling it with symbols.

IT2 Tx Buffer : each time the ST75C502 frees a buffer, this interrupt is generated.

IT3 Rx Buffer: each time the ST75C502 has filled a buffer, this interrupt is generated.

IT4 Status Byte : the modem status byte has changed and has to be checked by the controller.

IT6 Command Acknowledge : the ST75C502 has read the last command entered by the host, incremented the command counter COMACK, and is ready for a new command.

ITSRCR	x	D6	x	D4	D3	D2	D1	D0

D0 = 1 IT0 Pending
D1 = 1 IT1 Pending
Dn = 1 ITn Pending

ITMASK	D7	D6	x	D4	D3	D2	D1	D0

D7 and D0 = 1 IT0 Enabled
D7 and D1 = 1 IT1 Enable
D7 and Dn = 1 ITn Enabled

VI.1.3 - Host Interface Summary

Address (hex)	Description	Size (Byte)	Mnemonic
COMMAND AREA			
$00	Command	1	COMSYS
$01-$04	Command Parameters	4	COMPAR[0..3]
REPORT AREA			
$05	Acknowledge Counter	1	COMACK
$06-$07	Report	2	COMREP[0..1]
STATUS AREA			
$08	Error Status	1	SYSERR
$09	General Status	2	STATUS[0..1]
$0B	Quality Monitor	1	STAQUA
$0C-$0E	Optional Report	3	STAOPT[0..2]
BULK DELAY AREA			
$OF	Symbol Buffer Status	1	SYMSTA
$10-$11	Symbol Rx Buffer Pointer	2	SYMADR[0..1]
$12-$13	Symbol Tx Buffer Pointer	2	SYMADT[0..1]
$14-$1B	Symbol Buffer	8	SYMBUF[0..7]
DATA AREA			
$1C	Data Rx Buffer 0 Status	1	DTRBS0
$25	Data Rx Buffer 1 Status	1	DTRBS1
$2E	Data Tx Buffer 0 Status	1	DTTBS0
$37	Data Tx Buffer 1 Status	1	DTTBS1
$1D-$24	Data Rx Buffer 0	8	DTRBF0[0..7]
$26-$2D	Data Rx Buffer 1	8	DTRBF1[0..7]
$2F-$36	Data Tx Buffer 0	8	DTTBF0[0..7]
$38-$3F	Data Tx Buffer 1	8	DTTBF1[0..7]
INTERRUPT AREA			
$40-$46	Reset Interrupt Register	7	ITREST[0..6]
$4F	Interrupt Mask Registe	1	ITMASK
$50	Interrupt Source Register	1	ITSRCR

VI.2 - Command Set

The Command Set has the following attractive features :

- user friendly with easy to remember mnemonics.
- possibility of straight forward expansion with new commands to suit specific customer requirements.
- easy upgrade of existing software using previous modem based SGS-THOMSON products.

The command set has been designed to provide the necessary functional control on the ST75C502. Each command is classified according to its syntax and the presence/absence of parameters. In the case of a parametric command, parameters must first be written into the dual port RAM before the command is issued. Acknowledge and error report is issued for each command entered.

VI.2.1 - Command Set Summary

VI.2.1.1 - Operational Control Commands

INIT Initialize. Initialize the modem chipset. Set all parameters to their default values and wait for commands of the control processor. Parametric command.

IDT Identify. Return the product identification code. Non parametric command.

SLEEP Turn to Low Power Mode. The modem engine issues a control signal to the MAFE in order to switch to Sleep Power Mode, then switches itself into Sleep Power Mode. Non parametric command.

HSHK Handshake. Begins the handshake sequence. The modem chipset carries all the steps defined in the ITU-T recommendations. A status report indicates to the control processor the state of the handshake and the final negotiated transmission bit rate. This command only applies to modes where a handshake sequence is defined. A CONF command must have been issued prior to the use of HSHK. Non parametric command.

RTRA Retrain. Start sending the retrain sequence as specified in the ITU-T recommendation. This command only applies to modes where a retrain sequence is defined. In V.32bis, this command also initiates the rate negotiation sequence. Parametric command.

CSE Clear Status Error. Selectively clears the Error status byte SYSERR. Parametric command.

SETGN Set gain. This command sets the global gain factor, which is used for the transmit samples. Parametric command.

STOP FAX Stop. Stop FAX half duplex transmitter. Non parametric command.

SYNC FAX Synchronize. Start/Stop of FAX half duplex receiver. Parametric command.

VI.2.1.2 - Data Communication Commands

XMIT Transmit data. Enable/disables the transmission of data in parallel mode. After a XMIT command, the ST75C502 sends the data contained in its dual port RAM. Parametric command.

SERIAL This command selects the data source, i.e. either parallel or serial. The parallel mode uses a part of the dual port RAM as a double buffer. The serial mode uses the serial synchronous I/O. Parametric command.

VI.2.1.3 - Digital Loop Back Commands

V54 V.54 Digital Loop Back. Enables/Disables the transmission and reception of V.54 patterns. This command must be used only in V.32 bis or V.32 mode. Parametric command.

V22L2 V.22/V.22 bis Digital Loop Back. Enables/Disables the transmission and reception of V.22 Loop 2 patterns. This command must be used only in V.22 bis or V.22 mode. Parametric command.

VI.2.1.4 - Memory Handling Commands

MW Memory Write. This command is used to write an arbitrary 16-bit value into the writable memory location currently specified by a parameter. Parametric command.

MR Memory Read. This command allows the controller to read any of the RAM locations without interrupting the processor. Parametric command.

CR Complex Read. This command allows the controller to read at the same time the real and imaginary part of a complex value stored in a double RAM location. This feature is very interesting for eye pattern software control as well as for equalization monitoring. This command insures that the real and imaginary part are sampled in the memory at the same time (integrity). Parametric command.

VI.2.1.5 - Configuration Control Commands

CONF Configures. This command configures the modem chipset for data transmission and handshake procedures (if any) in any of the supported modes. The transmission parameters are set to their default values and can be modified with the MODC command. This command also defines the parameters in the case of an automatic standard recognition and the boundaries of the speed negotiation. Parametric command.

MODC Modify Configuration. This command allows modification of part of the parameters set up by the CONF command. Parametric command.

BULK Define Symbol Bulk Management. This command selects the dual port RAM symbol management, in V.32bis and V.32 modes. Parametric command.

DOSR Define Optional Status report. This command allow the modification of the optional status report located in the status area of the dual port RAM. One can thus select a particular parameter to be monitored during all modes of operation. Parametric command.

DSIT Define Status Interrupt. This command allows the programmation of the status word bit that will generate an Interrupt to the controller. Parametric command.

PPS Parallel Port Set. This command allows the modification of the parallel port configuration. Each of the four bits of this port can be programmed either as an input or an output. Parametric command.

PPR Parallel Port Read. This command reads the value of the 4-bit parallel port. The value is read whether it is an input or not. Non parametric command.

PPW Parallel Port Write. This command writes a 4-bit value into the parallel port. The bits are masked according to their input/output status. Parametric command.

VI.2.1.6 - MAFE Control Commands

WMR Write MAFE register. Causes the DSP to write a parameter into a MAFE register. Parametric command.

VI.2.1.7 - Tone Generation Commands

TONE Select Tone. Programs the tone generator(s) for the desired default tone(s). Additional mnemonics provide quick programming of DTMF tones or other currently used tones. Parametric command.

DEFT Define Tone. Programs the tone generator(s) for arbitrary tone synthesis. Parametric command.

TGEN Tone Generator Control. Enables or disables the tone generator(s). Parametric command.

IV.2.1.8 Tone Detection Commands

TDRC Read coefficients of tone detection cell. Parametric command.

TDWC Write coefficients of tone detection cell. Parametric command.

TDRW Read wiring of tone detection cell. Parametric command.

TDWW Write wiring to tone detection cell. Parametric command.

TDZ Clear the values of tone detection cell. Parametric command.

VI.2.2 - Command Set Short Form

Mnemonic	Value	Description
XMIT	0X01	**R**eceive/**T**rans**MIT** data
SETGN	0X02	**SET GaiN**
SLEEP	0X03	Low Power mode
HSHK	0X04	**H**and**SH**a**K**e
RTRA	0X05	**R**e**TRA**in
INIT	0X06	**INIT**ialization
SERIAL	0X07	**SERIAL** mode
CSE	0X08	**C**lear **S**tatus **E**rror
MR	0X10	**M**emory **R**ead
CR	0X11	**C**omplex **R**ead
MW	0X12	**M**emory **W**rite
DSIT	0X13	**D**efine **S**tatus word **I**n**T**errupt
IDT	0X14	**ID**en**T**ify
PPS	0X15	**P**arallel **P**ort **S**et
PPR	0X16	**P**arallel **P**ort **R**ead
PPW	0X17	**P**arallel **P**ort **W**rite
JSR	0X18	**J**ump to **S**ub **R**outine
CALL	0X19	CALL a sub routine
CONF	0X20	**CONF**igure
MODC	0X21	**MOD**ify **C**onfiguration
BULK	0X22	Define symbol **BULK** management
V54	0X23	Enable/Disable **V.54**
V22L2	0X24	Enable/Disable **V.22 L**oop**2**
STOP	0X25	FAX **STOP** Transmitter
SYNC	0X26	FAX **SYNC**hronize Receiver
DOSR	0X0A	**D**efine **O**ptional **S**tatus **R**eport
WMR	0X0B	Write **M**afe **R**egister
TONE	0X0C	Select **TONE**
TGEN	0X0D	**T**one **GEN**erator control
DEFT	0X0E	**DEF**ine **T**one
TDRC	0X1A	**T**one **D**etect **R**ead **C**oefficient
TDWC	0X1C	**T**one **D**etect **W**rite **C**oefficient
TDRW	0X1B	**T**one **D**etect **R**ead **W**iring
TDWW	0X1D	Tone **D**etect **W**rite **W**iring
TDZ	0X1E	**T**one **D**etect **Z**ero cell

VI.2.2.1 - Miscellaneous Commands

CALL Call a Subroutine. Call a Subroutine with one parameter.

JSR Call a low level Subroutine. Call an internal subroutine with one parameter.

VI.3 - Status - Reports

VI.3.1 - Status

The ST75C502 has a dedicated status reporting area located in its dual port RAM. This allows a continuous monitoring of the status variables without interrupting the DSP.

The first status byte gives the error status. Issuing of an error status can be also flagged by a maskable interrupt for the controller. The signification of the error codes is given in Annexe B.

The second and third status bytes give the general status of the modem. This two byte status can generate, when a change occurs, an interrupt to the controller; each bit of that two byte word can be masked independently.

The fourth byte gives, in real time, a measure of the reception quality. This information may be used by the controller for retrain purpose.

Three other locations are dedicated for custom status reporting. This status includes, for example, the handshake phase, the negotiated data rate, and other items described in Annexe B. The controller can program the ST75C502 for a real time monitoring of any of its internal RAM location. High byte or low byte of any word can thus be monitored.

VI.3.2 - Reports

The ST75C502 features an acknowledge and report facility. The acknowledge of a command is monitored by a counter COMACK located in the dual port RAM. Each time a command is executed from the command area, the ST75C502 will increment this counter. For instance, when a MR (Memory Read) command is issued, the data is first written in the report area, and the counter is incremented afterwards. This way of processing insures the data integrity as well as an additional synchronization between the controller and the data pump.

VI.4 - Data Exchange

The ST75C502 accepts two kinds of data exchange : Parallel synchronous through the DUAL RAM or SERIAL synchronous. Detailed description of the Data Buffer Exchange modes of operation is available in Appendix H.

VI.4.1 - Parallel Data Mode

VI.4.1.1 - Transmit

The controller must first fill at least the first buffer of data (Tx Buffer 0) with the bits to be transmitted. In order to perform this operation, the controller must first check the Tx Buffer 0 status word DTTBS0. If this buffer is empty, the controller fills the data buffer locations (up to 8 bytes), and then writes in DTTBS0 the number of bits contained in the buffer. The controller can then either proceed with the second buffer or initiate the transmission with a XMIT command.

The ST75C502 copies the contents of the data buffer and then clears the buffer status word in order to make it again available. The number of bytes specified by the status word is then queued for transmission. The process goes on with the two

buffers until an XMIT command stops the transmission. After the finishing XMIT command has been issued, the last buffers are emptied by the ST75C502.
Error occurs when both buffers are empty while the transmit byte queue is also empty. Error is signalled with an interruption to the controller through the SYSERR register.

VI.4.1.2 - Receive

The controller should take care of releasing the Rx buffers before the Data Carrier Detect goes true. This is made by writing a zero in the Rx Buffer Status 0 and 1. The ST75C502 then fills the first buffer, and once filled sets the status word with the number of bytes received. It then takes control of the second buffer and operates in the same way. The controller must check the status of the buffers and empty them. Once the data is read, the controller must release the used buffer and wait for the next buffer to be full. Interrupts are available for an additional flagging of these events.
Error occurs when both buffers are declared full, and incoming bytes still arrive from the line.
Synchronous Data Buffer Exchanges are described in Annex H.

VI.4.2 - Serial Exchanges

The second mode of operation for data exchanges is the Serial Synchronous Mode. In this mode, the data I/O is made through a pair of dedicated hardware pins (DR2, DX2).

VI.4.3 - Mafe Clocks

The MAFE generates all the transmit and receive clocks necessary for the modem application, some of them are to be also connected to the ST75C502 (see Table paragraph III.5 - MAFE INTERFACE). For more detailed information, please, refer to the ST7544 Data Sheet.

Table 1 : Modem Modes

Mode	Modulation	Carrier Frequency (Hz)	Data Rate (Bps)	Baud or symbol per second	Bits per symbol	Constellation points	TxCLK	RxCLK
V.32bis	QAM TCM	1800	14400 12000 9600 7200 4800	2400	6 5 4 3 2	128 64 32 16 4	14400 12000 9600 7200 4800	idem TxCLK
V.32	QAM TCM	1800	9600 4800	2400	4 2	32, 16 4	9600 4800	idem TxCLK
V.22bis originate	QAM	1200	2400 1200	600	4 2	16 4	2400 1200	idem TxCLK
V.22bis answer	QAM	2400	2400 1200	600	4 2	16 4	2400 1200	idem TxCLK
V.22 or Bell 212 originate	DPSK	1200	1200	600	2	4	1200	idem TxCLK
V.22 or Bell 212 answer	DPSK	2400	1200	600	2	4	1200	idem TxCLK
V.23 answer	FSK	1300, 2100	1200	1200	1	-	7200	9600
V.23 originate	FSK	390, 450	75	75	1	-	7200	9600
Bell 103 originate	FSK	1270, 1070	300	300	1	-	7200	9600
Bell 103 answer	FSK	2225, 2025	300	300	1	-	7200	9600
V.21 originate	FSK	980, 1180	300	300	1	-	7200	9600
V.21 answer	FSK	1650, 1850	300	300	1	-	7200	9600
V.33	QAM TCM	1800	14400 12000	2400	6 5	128 64	14400 12000	idem TxCLK
V.17	QAM TCM	1800	14400 12000 9600	2400	6 5 4 3	128 64 32 16	14400 12000 9600 7200	idem TxCLK
V.29	QAM	1700	9600 7200 4800	2400	4 3 2	16 8 4	9600 7200 4800	idem TxCLK
V.27ter	DPSK	1800	4800 2400	1600 1200	3 2	3 2	4800 2400	idem TxCLK
V.21 ch 2	FSK	1650, 1850	300	300	1	-	300	300

APPENDIX A : COMMAND SET DESCRIPTION

Commands are presented according to the following form :

COMMAND - Command name meaning

Opcode : hexadecimal digit

X	X	X	X	X	X	X	X

Synopsis

Short description of the functions performed by the command

Parameters

Field	Byte	Pos.	Value	Definition
Name	X	a..b		Explanation of the parameter
			xx *	Default value

Field : Name of the addressed bit field.
Byte : Index (or address in the dual port RAM) of the parameter byte (from 1 to 4).
Pos. : Bit field position inside the parameter byte. Can either be a single position (from 0 to 7, 0 being LSB) or a range.
Value : Possible values for the bit (resp. bit field). *range* means all values are allowded. A value followed by a star means a default value. Values are expressed either under the form of a bit string, or under hexadecimal format.

Command :

BULK - Define Symbol Management

Opcode : 22

0	0	1	0	0	0	1	0

Synopsis

BULK allows the use of the DUAL RAM symbol area. This additional task into host firmware is only needed in V.32/V.32bis mode. This mode of operation is mandatory.

In this command the user sets the virtual memory base address and the top memory address (the base address must be on a 8 byte boundary and the top address on a 8 byte boundary - 1 eg : 0x67FF) of the MCU memory space reserved for BULK DELAY symbols storage.

Parameters

Field	Byte	Pos.	Value	Definition
BA_ADDR_L	1	7..0		Low byte of the base address
BA_ADDR_H	2	7..0		High byte of the base address
TO_ADDR_L	3	7..0		Low byte of the top memory address
TO_ADDR_H	4	7..0		High byte of the top memory address

(required capacity in MCU memory space is 2400 x d (d = BULK DELAY in seconds))

CALL - Call a subroutine

Opcode : 19

0	0	0	1	1	0	0	1

Synopis

CALL allows to execute a part of the DSP firmware with a specific argument.

Parameters

Field	Byte	Pos.	Value	Definition
C_ADDR_L	1	7..0		Low byte of the call address
C_ADDR_H	2	7..0		High byte of the call address
C_DATA_L	3	7..0		Low byte of the argument
C_DATA_H	4	7..0		High byte of the argument

CONF - Configure for operations

Opcode : 20

0	0	1	0	0	0	0	0

Synopsis

CONF allows the complete definition of the ST75C502 operation, including the mode of operation (Tone, Data Transmit, FAX Transmit, Voice Transmit, Voice Receive, DTMF Receive, ...) and the Modem Parameters (Standard, Speed, ...).

Parameters

Field	Byte	Pos.	Value	Definition
CONF_OPER	1	3..0	-	Mode of operation, see below
CONF_ANAL	1	4	0 1	Normal mode Analog loop back
CONF_PSTN	1	5	0 1	PSTN (carrier detect set to -43/-48dBm) Lease line (carrier detect -33/-38dBm)
CONF_AO	1	6	0 1	Answer mode Originate mode
CONF_MODE	2	5..0	0 1 2 3 4 5 6 7 8 9 A B C D Other	Automode Bell 103 Bell 212A V.21 V.23 V.22 V.22bis V.27ter V.29 V.17 V.32 V.32bis V.33 V.21 channel 2 Reserved

Parameters (continued)

Field	Byte	Pos.	Value	Definition
CONF_TXEQ	2	7..6	0 1 2 3	No transmit equalizer Transmit equalizer #1 (1/2 of M1020) Transmit equalizer #2 (1/2 of M1040) Reserved
CONF_QAM	3	0	0 1	QAM/DPSK only (Automode) FSK allowed (Automode)
CONF_TCM	3	1	0 1	Treillis coding not allowed (V.32 only) Treillis coding allowed (V.32bis, V.32)
CONF_SP0	3	7..2	xxxx01 xxxx0x xxx10x xx1x0x x1xx0x 1xxx0x	300 bps allowed (V.21, Bell 103) Reserved (must be set to 0) 1200 bps allowed (V.22, V.22bis, V.23, Bell 212A) 2400 bps allowed (V.22bis, V.27) 4800 bps allowed (V.32bis, V.32, V.29, V.27) 7200 bps allowed (V.32bis, V.29, V.17)
CONF_SP1	4	2..0	xx1 x1x 1xx	9600 bps allowed (V.32bis, V.32, V.29, V.17) 12000 bps allowed (V.32bis, V.33, V.17) 14400 bps allowed (V.32bis, V.33, V.17)

According with the 4 first bits of the CONF_OPER the ST75C502 is put into the following mode of operation.

CONF_OPER	Transmit	Receive	Number of tone detectors available
0000*	Tones	Tones	16
0010	Voice	Tones	16
0100	Tone	DTMF	4 (1)
0110	Voice	DTMF	4 (1)
1000	Tones	Voice	16
1010	Voice	Voice	16
1111	**Modem**	**Modem**	0 (2)
Other	Not allowed	Not allowed	-

Notes : **1.** 12 of the tone detectors are used by the DTMF detector.
2. When in Data Modem Mode, the number of tone detectors is set to 0. The user can set it up to 2 if the SERIAL link is used (instead of the parallel data mode). it is set to 2 in FAX Receive Mode, and 8 in V.21 channel 2 mode. To modify the number of tone detectors available, the user must overwrite the _NTDCELL DSP internal variable with a MW command (refer to "RAM mapping Application Note").
3. Unless otherwise required Tx equalizer #1 should be selected for better compromize on the general switched telephone network.

CR - Complex read

Opcode : 11

0	0	0	1	0	0	0	1

Synopsis

CR allows the reading of a complex parameter. The parameter specifies the parameter address (for the real part : the imaginary part is next location). CR returns the high byte value of both real and imaginary part of the addressed complex parameter.

Parameters

Field	Byte	Pos.	Value	Definition
CR_ADDR_L	1	7..0		Low byte of the 16-bit address
CR_ADDR_H	2	7..0		High byte of the 16-bit address

CSE - Clear error status

Opcode : 08

0	0	0	0	1	0	0	0

Synopsis

CSE is used to clear the ST75C502 error status SYSERR byte. It is also used as an acknowledge to the error condition handler.

Parameters

Field	Byte	Pos.	Value	Definition
ERR_MASK	1	7..0		Error mask . See report appendix for detailed meaning.

DEFT - Define arbitrary tone

Opcode : 0E

0	0	0	0	1	1	1	0

Synopsis

DEFT programs one of the four tone generator for arbitrary tone generation. The parameter is the frequency of the generated tone in Hertz between 0 and 3600 Hz (expressed in hexadecimal).

Parameters : Example 1000 Hz is represented by 03E8

Field	Byte	Pos.	Value	Definition
TONE_GEN_SL	1	1..0		Index of the tone generator (0..3)
TONE_FREQ_L	2	7..0		Low byte of the frequency
TONE_FREQ_H	3	7..0		High byte of the frequency (internally masked with 0F)
TONE_SCALE	4	7..0		Amplitude scaling factor (high byte) 3F gives the nominal amplitude

DOSR - Define optional status report

Opcode : 0A

0	0	0	0	1	0	1	0

Synopsis

DOSR specifies the address of the RAM variables to be monitored in the 3 locations STAOPT[0..2] of the dual port RAM. It also specifies the assignment within the 3 locations.

Parameters

Field	Byte	Pos.	Value	Definition
STA_OPT_ASS	1	2..0		Index of the STAOPT destination
STA_OPT_ADL	2	7..0		Low byte of source address
STA_OPT_ADH	3	3..0		High byte of source address
STA_OPT_HL	3	7	0 1	Select low byte of source Select high byte of source

DSIT - Define status interrupt

Opcode : 13

0	0	0	1	0	0	1	1

Synopsis

DSIT specifies the bit mask used with the **STATUS[0]** or **STATUS[1]** byte to generate an interrupt **IT4** to controller. Each time a bit change will append in the general status words, assuming the corresponding bit mask will be set, an interrupt will be generated.

Parameters

Field	Byte	Pos.	Value	Definition
STA_IT_MSK0	1	7..0		Status 0 Bit Mask pattern
STA_IT_MSK1	2	7..0		Status 1 Bit Mask pattern

Note : The default IT status is 0X3F for STATUS [0] and 0XFF for STATUS [1].

HSHK - Handshake

Opcode : 04

0	0	0	0	0	1	0	0

Synopsis

HSHK is used to command the ST75C502 to begin the handshake sequence processing. The progress of the handshake is reported to the control processor.

Parameters : non parametric command

IDT - Identify

Opcode : 14

0	0	0	1	0	1	0	0

Synopsis

IDT returns the ST75C502 Harware and Software release number. See Appendix B, paragraph I.2.2.

Parameters : non parametric command

Bits 15 to 12 represent the product identity number. For the ST75C502 this is 0
Bits 11 to 4 represent the product software release
Bits 3 to 0 represent the software sub release

INIT - Initialization

Opcode : 06

0	0	0	0	0	1	1	0

Synopsis

INIT forces the ST75C502 to reset all parameters to their default values and restart operations as after a Hardware Reset. It clears all the internal RAM, the DUAL RAM and restarts in Tone mode.

Parameters

Field	Byte	Pos.	Value	Definition
INIT_MODE	1	0	0	"Cold initialization" : initialize all variables and ST7544 chip. Maximum duration 500ms.
			1	"Warm initialization" : initialize only the variables. Maximum duration 10ms.

Notes : **1.** This command makes a software reset of the ST75C502 and so cannot have the regular handshake protocol. It does not increment the COMACK, nor generate an Interrupt.

2. The INIT command does not affect the contains of the ITMASK and ITSRCR registers.

JSR - Call a low level subroutine

Opcode : 18

0	0	0	1	1	0	0	0

Synopsis

JSR allows execution of a part of the DSP firmware with specific argument.

Parameters

Field	Byte	Pos.	Value	Definition
C_ADDR_L	1	7..0		Low byte of the call address
C_ADDR_H	2	7..0		High byte of the call address
C_DATA_L	3	7..0		Low byte of the argument
C_DATA_H	4	7..0		High byte of the argument

MODC - Modify configuration

Opcode : 21

0	0	1	0	0	0	0	1

Synopsis

MODC allows modification of the configuration for special purposes. This command has no effect while in data mode, the parameters are just sampled when starting to transmit or receive.

Parameters

Field	Byte	Pos.	Value	Definition
MODC_SH	1	6	0* 1	Normal training sequence Short training (1) sequence
MODC_V22G	2	1..0	00* 01 10	No guard tone 1800Hz guard tone 550Hz guard tone
MODC_FPT	2	3..2	00* 10	No echo protection tone Long echo protection tone (180ms) (FAX only)
MODC_NOTA	2	4	0*	Answer mode : generate answer tone for handshake Originate mode : wait answer tone for handshake
			1	Answer mode : do not generate answer tone for handshake Originate mode : do not wait answer tone for handshake
MODC_NOSA	2	6	0* 1	Cut answer tone when receiving AA (V.32bis, V.32) Continue answer tone when receiving AA
MODC_NOQA	2	7	0* 1	Enable V.32bis handshake on quality Disable handshake on quality

Note1 : Short train sequence must be preceded by at least one normal training sequence.

MR - Memory read

Opcode : 10

0	0	0	1	0	0	0	0

Synopsis

MR allows the reading of a 16-bit parameter. The parameter specifies the parameter address.

Parameters

Field	Byte	Pos.	Value	Definition
MR_ADDR_L	1	7..0		Low byte of the 16-bit address
MR_ADDR_H	2	7..0		High byte of the 16-bit address

MW - Memory write

Opcode : 12

0	0	0	1	0	0	1	0

Synopsis

MW allows the writing of a 16-bit parameter. The parameter specifies the address, as well as the value, to be transferred.

Parameters

Field	Byte	Pos.	Value	Definition
MW_ADDR_L	1	7..0		Low byte of the 16-bit address
MW_ADDR_H	2	7..0		High byte of the 16-bit address
MW_VALUE_L	3	7..0		Low byte of the 16-bit value
MW_VALUE_H	4	7..0		High byte of the 16-bit value

PPR - Read parallel port

Opcode : 16

0	0	0	1	0	1	1	0

Synopsis

Read parallel port. The values of the 4-bit parallel port is read, whether the port is configured in input or in output.

Parameters : non parametric command

PPS - Parallel port set

Opcode : 15

0	0	0	1	0	1	0	1

Synopsis

Configure parallel port. Each of the 4 pins of the parallel port can be either programmed for input or for output.

Parameters

Field	Byte	Pos.	Value	Definition
PP_IO0	1	0	0* 1	Pin 0 programmed as input Pin 0 programmed as output
PP_IO1	1	1	0* 1	Pin 1 programmed as input Pin 1 programmed as output
PP_IO2	1	2	0* 1	Pin 2 programmed as input Pin 2 programmed as output
PP_IO3	1	3	0 1*	Pin 3 programmed as input Pin 3 programmed as output

Note : Pin 3 is reserved for MAFE control and therefore must be programmed as an output.

PPW - Parallel port write

Opcode : 17

0	0	0	1	0	1	1	1

Synopsis

Write to the parallel port. This operation will be effective only if the bits are programmed as outputs.

Parameters

Field	Byte	Pos.	Value	Definition
PP_VAL0	1	0		Pin 0 logical value
PP_VAL1	1	1		Pin 1 logical value
PP_VAL2	1	2		Pin 2 logical value
PP_VAL3	1	3	1	Pin 3 logical value must be set to 1

RTRA - Retrain

Opcode : 05

0	0	0	0	0	1	0	1

Synopsis

RTRA is used to force the ST75C502 to initiate a retrain sequence on the channel. The parameter determines the target speed for the retrain.

Parameters

Field	Byte	Pos.	Value	Definition
RTRA_NEGO	1	0	0 1	Retrain (V.22bis, V.32, V.32bis) Rate Negotiation (V.22bis, V.32bis)
RTRA_NEGO	1	1	1 0	Treillis coding enabled Treillis coding not enabled
RTRA_1200	1	4	0 1	1200 bps speed not allowed 1200 bps speed allowed
RTRA_2400	1	5	0 1	2400 bps speed not allowed 2400 bps speed allowed
RTRA_4800	1	6	0 1	4800 bps speed not allowed 4800 bps speed allowed
RTRA_7200	1	7	0 1	7200 bps speed not allowed 7200 bps speed allowed
RTRA_9600	2	0	0 1	9600 bps speed not allowed 9600 bps speed allowed
RTRA_12000	2	1	0 1	12000 bps speed not allowed 12000 bps speed allowed
RTRA_14400	2	2	0 1	14400 bps speed not allowed 14400 bps speed allowed

SERIAL - Select serial or parallel mode

Opcode : 07

0	0	0	0	0	1	1	1

Synopsis

SERIAL defines the data path, i.e. either serial or parallel.

Parameters

Field	Byte	Pos.	Value	Definition
TX_SDATA	1	0	0* 1	Use serial link for Tx data Use parallel link for Tx data
RX_SDATA	1	1	0* 1	Use only serial link for Rx data Use also parallel link for Rx data

Note : The received bits always go to output pin DX2, even when the Rx_SDATA bit is set.

SETGN - Set output gain

Opcode : 02

0	0	0	0	0	0	1	0

Synopsis

SETGN is a command which sets the scaling factor of the transmit samples. It is used for setting the output level or for setting the level of the tone generators. The gain value is given in the form of a 2's complement 16-bit value.

Parameters

Field	Byte	Pos.	Value	Definition
GAIN_L	1	7..0	range FF*	Low byte of the 16-bit gain value
GAIN_H	2	7..0	range 7F*	Hight byte of the 16-bit gain value

Example :

Gain (dB)	Gain (Hex)	Gain (dB)	Gain (Hex)	Gain (dB)	Gain (Hex)
0	7FFF	-5	47FA	-10	287A
-1	7214	-6	4026	-11	2413
-2	65AC	-7	392C	-12	2026
-3	5A9D	-8	32F5	-13	1CA7
-4	50C3	-9	2D6A	-14	198A

SLEEP - Turn to low power mode

Opcode : 03

0	0	0	0	0	0	1	1

Synopsis

SLEEP is used to force the ST75C502 to turn to low power mode.

Parameters : non parametric command

Note : When receiving this command the ST75C502 will stop processing and so cannot have the regular handshake protocol. It does not increment the COMACK, nor generate an Interrupt.

STOP - FAX stop transmitter

Opcode : 25

0	0	1	0	0	1	0	1

Synopsis

STOP is used, in FAX modes, to force the ST75C502 to turn-off the transmitter in accordance with the corresponding ITU-T V.33 / V.17 / V.29 / V.27ter / V.21 channel 2 recommendations.

Parameters : non parametric command

Note : When receiving this command the ST75C502 will stop sending regular data. In parallel mode this command must be preceded by a **XMIT** stop command. After receiving the **STOP** command the ST75C502 will wait until all the transmit buffers are sent commencing with the stop sequence.

SYNC - FAX synchronize the receiver

Opcode : 26

0	0	1	0	0	1	1	0

Synopsis

SYNC is used, in FAX modes, to force the ST75C502 to start/stop the receiver in accordance with the corresponding ITU-T V.33 / V.17 / V.29 / V.27ter / V.21 channel 2 recommendations.

As soon as the ST75C502 receives the **SYNC** start command it sets its receiver to detect the FAX synchronization signal.

This commdand is the equivalent **HSHK** command for the receiver.

Parameters

Field	Byte	Pos.	Value	Definition
RX_SYNC	1	0	0* 1	Stop receiver Start receiver synchronization

TDRC - Tone detector read coefficient

Opcode : 1A

0	0	0	1	1	0	1	0

Synopsis

TDRC read one coefficient of the selected tone detector cell.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	3..0	0..F	Tone detector cell number
TD_C_ADDR	2	7..0	0..B 10 20 other	Biquad coefficient Energy coefficient Static level Reserved

The command answer is : low byte of coefficient followed by high byte of coefficient.

TDRW - Tone detector read wiring

Opcode : 1B

0	0	0	1	1	0	1	1

Synopsis

TDRW read wiring of the selected tone detector cell.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	3..0	0..F	Tone detector cell number
TD_W_ADDR	2	0	0 1 other	Biquad and energy input Comparator inputs Reserved

The command answer is :

a) if TD_W_ADDR = 0 :
   - first byte is the node number of signal connected to biquadratic filter input,
   - second byte is the node number of the signal connected to the energy estimator input.

b) if TD_W_ADDR = 1 :
   - first byte is the node number of signal connected to comparator negative input,
   - second byte is the node number of the signal connected to the comparator positive input.

TDWC - Tone detector write coefficient

Opcode : 1C

0	0	0	1	1	1	0	0

Synopsis

TDWC write one coefficient of the selected tone detector cell.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	3..0	0..F	Tone detector cell number
TD_C_ADDR	2	7..0	0..B 10 20	Biquad coefficient Energy coefficient Static level
TD_COEFL	3	7..0		Low byte of coefficient
TD_COEFH	4	7..0		High byte of coefficient

TDWW - Tone detector write wiring

Opcode : 1D

0	0	0	1	1	1	0	1

Synopsis

TDWW write wiring of the selected tone detector cell.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	3..0	0..F	Tone detector cell number
TD_W_ADDR	2	0	0 1	Biquad and energy input Comparator inputs

if TD_W_ADDR = 0 (select biquad and energy inputs)

Field	Byte	Pos.	Value	Definition
TD_W_ERN	3		0..3F	Energy estimator signal input
TD_W_BIQ	4		0..3F	Biquad filter signal input

if TD_W_ADDR = 1 (select comparator inputs)

Field	Byte	Pos.	Value	Definition
TD_W_CN	3		0..3F	Negative comparator signal input
TD_W_CP	4		0..3F	Positive comparator signal input

TDZ - Tone detector clear cell

Opcode : 1E

0	0	0	1	1	1	1	0

Synopsis

TDZ clears all internal variables of one Tone detector cell including filter local variables and energy estimator. This command must be sent after changing coefficients of a cell to avoid instability.

Parameters

Field	Byte	Pos.	Value	Definition
TD_CELL	1	3..0	0..F	Tone detector cell number

TGEN - Enable/disable tone generators

Opcode : 0D

0	0	0	0	1	1	0	1

Synopsis

TGEN causes the ST75C502 to enable or disable the four tone generators.

Parameters

Field	Byte	Pos.	Value	Definition
TONE_0_ENA	1	0	0* 1	Generator #0 disabled Generator #0 enabled
TONE_1_ENA	1	1	0* 1	Generator #1 disabled Generator #1 enabled
TONE_2_ENA	1	2	0* 1	Generator #2 disabled Generator #2 enabled
TONE_3_ENA	1	3	0* 1	Generator #3 disabled Generator #3 enabled

TONE - Predefined tones

Opcode : 0C

0	0	0	0	1	1	0	0

Synopsis

TONE programs the tone generators for the predefined tones. The tone generators #0 and eventually #1 are reprogrammed with this command. Eventualy the tone generator #0 and #1 are enabled. Using an argument not in the following table will disable tone generator #0 and #1.

Parameters

Field	Byte	Pos.	Value	Definition
TONE_SELECT	1	5..0	0	DTMF 0 (941 & 1336Hz)
			1	DTMF 1 (697 & 1209Hz)
			2	DTMF 2 (697 & 1336Hz)
			3	DTMF 3 (697 & 1477Hz)
			4	DTMF 4 (770 & 1209Hz)
			5	DTMF 5 (770 & 1336Hz)
			6	DTMF 6 (770 & 1477Hz)
			7	DTMF 7 (852 & 1209Hz)
			8	DTMF 8 (852 & 1336Hz)
			9	DTMF 9 (852 & 1477Hz)
			A	DTMF A (697 & 1633Hz)
			B	DTMF B (770 & 1633Hz)
			C	DTMF C (852 & 1633Hz)
			D	DTMF D (941 & 1633Hz)
			E	DTMF * (941 & 1209Hz)
			F	DTMF # (941 & 1477Hz)
			10	Answer Tone (2100Hz)
			11	Tone (1650Hz)
			12	Answer Tone (2225Hz)
			13	Tone (1300Hz)

V22L2 - V22 loop 2 generator/detector

Opcode : 24

0	0	1	0	0	1	0	0

Synopsis

V22L2 selects the transmission and detection of V.22/V.22bis patterns required for remote digital loop back as defined in the ITU-T specification. The STA_V22L bit in the STA_LOOP optional status word will follow the detection of the receiver setting. This command must only be used in V.22 or V.22bis modes.

Note that the STA_V22A bit (alternate ”1010” or ”0101”) in the STA_LOOP is always active.

Parameters

Field	Byte	Pos.	Value	Definition
V22L2_TX	1	1..0	00*	Data mode
			01	Transmit unscrambled ”1”
			10	Transmit scrambled ”1”
			11	Transmit scrambled ”1010”
V22L2_RX	2	0	0*	Detect unscrambled ”1”
			1	Detect scrambled ”1”

V54 - Generator/detector

Opcode : 23

0	0	1	0	0	0	1	1

Synopsis

V.54 selects the transmission and detection of V.54 patterns required for remote digital loop back as defined in the ITU-T specification. The STA_V54D bit in the STA_LOOP optional status word will follow the detection of the receiver setting. This command must only be used in V.32 or V.32bis modes.

When the transmit generator completes the required pattern it will continue to send the same sequence and set the STA_V54E bit in the STA_LOOP.

Parameters

Field	Byte	Pos.	Value	Definition
V54_TX	1	1..0	00* 01 10 11	Data mode Transmit 2048 V54 scrambled ”0” Transmit 1948 V54 scrambled ”1” Transmit 8192 V54 scrambled ”1”
V54_RX	2	1..0	00* 01 10 11	No V54 detection Reserved Detect 256 V54 scrambled ”0” Detect 256 V54 scrambled ”1”

XMIT - Start/stop transmission

Opcode : 01

0	0	0	0	0	0	0	1

Synopsis

XMIT enables or disables the transmission of the data according to the selected mode (serial or parallel).

Parameters

Field	Byte	Pos.	Value	Definition
TX_START	1	0	0* 1	Stop transmission Start transmission

WMR - Write MAFE Register

Opcode : 11

0	0	0	1	0	0	0	1

Synopsis

WMR allows the writing of a 8-bit parameter into one of the ST7544 MAFE chip register.

Parameters

Field	Byte	Pos.	Value	Definition
MWR_DATA	1	7..0		Byte od data
MWR_ADDR	2	1..0		Byte of the 2-bit address
MWR_RXTX	3	7..0	0 0	Acess Tx Register Access Rx Register

This command must be used to lock the Transmit clock on an external clock or the received clock :

WMR D0 02 00 Tx Clock locked on TxSCLK input Pin.
WMR F0 02 **00** Tx Clock locked on Rx Clock.
WMR C0 02 00 Tx Clock free running

APPENDIX B : STATUS DESCRIPTION

This appendix is dedicated to the ST75C502 reporting features. In the following sections are explained the command acknowledge process and the report and status definitions.

I - COMMAND ACKNOWLEDGE AND REPORT

I.1 - Command Acknowledge Process

The ST75C502 features an acknowledge process based on a counter COMACK. On power-on reset, this counter's value is set to 0. Each time a command is executed, the acknowledge counter COMACK is incremented. This allows a precise monitoring of the command entered and avoids command collision.

The acknowledge counter is incremented as soon as the command has been properly executed. Furthermore, the ST75C502 resets the value of the COMSYS register. The interruption IT6 is raised just after the counter is incremented.

In the case of a memory reading command (CR, MR or PPR), the process is slightly different. The command entered is executed, the report area is then filled and the acknowledge counter is incremented afterwards. This insures that the controller reads the value corresponding to its request. Figure B1 gives a flowchart of the command acknowledge process.

I.2 - Reports Specification

The report section of the Dual Port RAM is dedicated to memory reading. In response to a CR, MR, IDT or PPR command, the value to be read is transferred to the Report registers COMREP[0..1].

I.2.1 - CR Command

Issuing a CR command causes the ST75C502 to dump a specific memory location in complex mode. This instruction is particularly usefull for equalizer state analysis or for software eye-pattern display. The report area has this meaning :

RP7	RP6	RP5	RP4	RP3	RP2	RP1	RP0	COMREP[0]

IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0	COMREP[1]

RP7..RP0 is the MSB part of the 16-bit value of the real part and IP7..IP0 is the MSB part of the imaginary part. The CR command insures that the real and imaginary parts of the desired complex value are sampled internally at the same time. The address given in the parameter field of CR is the address of the real part.

I.2.2 - MR/TDRC/IDT/TDRW Commands

The report issued by the MR/TDRC command is followings the same rules as the CR. The report meaning is :

D7	D6	D5	D4	D3	D2	D1	D0	COMREP[0]

D15	D14	D13	D12	D11	D10	D9	D8	COMREP[1]

D15..D0 is the 16-bit value required by the MR/TDRC command.

In the case of IDT, D15..D12 contains the product identification (0 for ST75C502), D11..D8 contains the hardware revision identification and D7..D0 contains the software revision identification.

I.2.3 - PPR Command

The PPR command issues the following report :

0	0	0	0	PP3	PP2	PP1	PP0	COMREP[0]

PP0..PP3 are the values read on the 4 pins of the parallel port. The result doesn't take into acccount the fact that those pins are input or output pins.

II - STATUS

II.1 - Modem Status

The status of the ST75C502 is divided into 4 fields :
- the error status byte SYSERR that provides information about error. This status can trigger an IT0 interrupt,
- the general status byte STATUS[0] and STATUS[1] that contains all the modem signals. These status bytes can trigger an IT4 interrupt,
- the quality status STAQUA, that contains the quality of the received transmission,
- the optional status bytes STAOP[0], STAOP[1] and STAOP[2], that contains additional information regarding the ST75C502 operating mode. This default information can be changed to monitor any internal variables using the DOSR command.

All these infomations are updated on a baud basis :

Mode	Baud Rate (Hz) (2)
Tone, DTMF, Voice	2400
V.32bis, V.32	2400
V.22bis, V.22, Bell 212A	2400
V.21, Bell 103	2400
V.23	2400
V.27ter 2400bps	1200
V.27ter 4800bps	1600 (1)
V.29	2400
V.17, V.23	2400
V.21 channel 2	2400

Notes : 1. The tone detectors outputs are update 800 times by seconds.
2. This baud rate defines also, the maximum command rate. Each baud time the ST75C502 looks at the COMSYS location (Address $00) to see if a command have been send by the host processor. If the content of this location is different from zero the ST75C502 execute the command.

Starting at the address $08 the status area have the following format :

Add.	Name	Bit							
		7	6	5	4	3	2	1	0
$08	SYSERR	ERR_RTK	-	-	ERR_IPRM	ERR_IOCD	ERR_SYM	ERR_RX	ERR_TX
$09	STATUS0	STA_109F	STA_CLR	STA_RNEG	STA_RTRN STA_HR	STA_AT	STA_CCITT	STA_TIM	STA_H
$0A	STATUS1	HSHK_PHA							
$0B	STAQUA	Quality							
$0C	STAOP0	Depend on operating mode (see below)							
$0D	STAOP1								
$0E	STAOP2								

II.2 - Error Status

The error status is changed each time an error occurs. When the ST75C502 signals an error by setting one of the SYSERR bit, it generate an interrupt IT0. These bits can only be cleared by the host-controler using the CSE command.
The meaning of the different bits of the SYSERR byte is discribed below :

SYSERR		
Field	**Pos.**	**Meaning when set**
ERR_TX	0	Transmit buffer underflow. Loss of synchronisation between the host and ST75C502 transmit data buffer managment
ERR_RX	1	Receive buffer overflow. Loss of synchronisation between the host and ST75C502 receive data buffer managment
ERR_SYM	2	Symbol buffer synchronization error (V.32, V.32bis)
ERR_IOCD	3	Incorrect CCI command
ERR_IPRM	4	Incorrect parameter for the CCI command
ERR_RTK	7	Real time kernel error. ST75C502 not able to perform all its tasks within the Baud period (transmit or receive samples lost)

II.3 - Modem General Status

The modem general status word is composed of two bytes STATUS[0] and STATUS[1]. Any bit change can generate an IT4 interrupt. Using the DSIT command allows the selection of the corresponding bit that will generate an interrupt each time they will change. The default pattern is $3F for STATUS[0] and $FF for STATUS[1]. The different bits have the following meaning :

STATUS[0]		
Field	**Pos.**	**Meaning when set**
STA_109	0	ITU-T circuit 109 (carrier detect). Indicates that valid data are received. When 0 the output data RxD are clamped to constant mark. Valid only in modem mode.
STA_107	1	ITU-T circuit 107 (data set ready). Valid only in modem mode.
STA_106	2	ITU-T circuit 106 (clear to send). Indicates that the training sequence has been completed and that any data at TxD pin (serial mode) or in the transmit buffer (parallel mode) will be transmitted. Valid only in modem mode.
STA_RING	3	Ring detected. A ring signal (from 15Hz to 68Hz) is present at the RING pin. Valid only in tones modes. The precise frequency can be read in the optional status byte STAOP2. The detection time is 1 period of the ring signal. The detection lost time is 20ms after the last transition on the ring signal.
STA_CPT0	4	Call progress tone detector #0. Low pass filter 650Hz. Valid only in tones modes.
STA_CPT1	5	Call progress tone detector #1. High pass filter 600Hz. Valid only in tones modes.
STA_CPT10	6	Signal in filter #0 is higher than #1. Valid only in tones modes.
STA_109F	7	Fast carrier detect. Valid only in FAX modem mode.

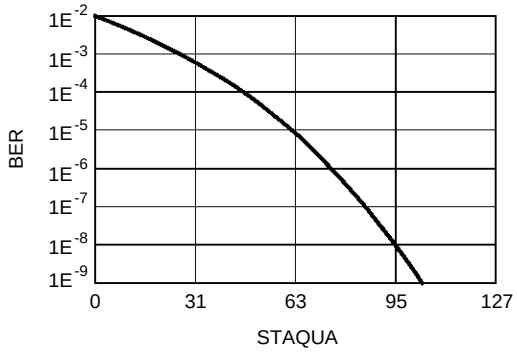
STATUS[1]		
Field	**Pos.**	**Meaning when set**
STA_H	0	Transmit synchronization in progress. Valid only in modem mode.
STA_TIM	1	Handshake timeout. Valid only in data modem mode.
STA_CCITT	2	Originate mode or tone : 2100Hz versus 2225Hz detected Answer mode : 1800Hz (AA signal) versus 2225Hz detected
STA_AT	3	Answer tone detect, either 2100Hz (or 1800Hz) or 2225Hz. This bit allows the sampling of the STA_CCITT bit.
STA_RTRN **STA_HR**	4	V.32bis, V.32, V.22bis : remote retrain detected Fax mode (including V.21 channel 2) : receiver synchronization in progress
STA_RNEG	5	V.32bis, V.32, V.22bis : remote rate negociation detected
STA_CLR	6	V.32bis, V.32 : cleardown detected
STA_DTMF	7	DTMF digit detect. The digit itself is available in the optional status byte STAOP2. Valid only in DTMF receive mode.

II.4 - Quality Status

The quality byte STAQUA monitors an evaluation of the line quality. It is updated once per baud and its value ranges from 127 (perfect quality) to 0 (terrible quality).

This value is automatically adjusted according to the current receiving mode (not valid in FSK modes).

Refer to the following chart to convert the value into its bit error rate equivalence.



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II.5 - Optional Status

According to the operating mode of the ST75C502 the optional status is displaying different informations.

The optional status are automatically reprogrammed after each CONF command with the address of the variables to monitor according with the operating mode selected (CONF_OPER). After the CONF command the user must overwrite this default programming by using the DOSR command. In order to change the default setup ; please refer to the "RAM Mapping ApplicationNlote" to obtain the addresses of the DSP internal variables.

II.5.1 - Default Optional Status in Tone Mode

While in tone mode the format of the STAOP word is as follows :

Add.	Name	Bit							
		7	6	5	4	3	2	1	0
$0C	STAOP0	TDT7	TDT6	TDT5	TDT4	TDT3	TDT2	TDT1	TDT0
$0D	STAOP1	TDT15	TDT14	TDT13	TDT12	TDT11	TDT10	TDT9	TDT8
$0E	STAOP2	RING_PERIOD (1)							

Notes : 1. RING_PERIOD is valid when the bit 3 of the STATUS[0] (STA_RING) goes high). This value is updated at each falling edge of the RING signal. The RING_PERIOD value must be divided by 2400 to obtain the period in seconds.
2. TDTx is the output of the tone detector x.

II.5.2 - Default Optional Status in DTMF Receiver Mode

While in DTMF receiver mode the format of the STAOP word is as follows :

Add.	Name	Bit							
		7	6	5	4	3	2	1	0
$0C	STAOP0	TDT7 (1)	TDT6 (1)	TDT5 (1)	TDT4 (1)	TDT3	TDT2	TDT1	TDT0
$0D	STAOP1	TDT15 (1)	TDT14 (1)	TDT13 (1)	TDT12 (1)	TDT11 (1)	TDT10 (1)	TDT9 (1)	TDT8 (1)
$0E	STAOP2	DTMF_DIGIT (2)							

Notes : 1. These cells are used by the DTMF detector.
2. DTMF_DIGIT is valid when the bit 7 of STATUS[1] (STA_DTMF) goes high. This value remains unchanged until a new DTMF digit is detected.

II.5.3 - Default Optional Status in Data Modem Mode

While in the DATA modem mode (V.32bis, V.32, V.22bis, V.22, V.23, V.21, Bell 212A or Bell 103) the format of the STAOP word is as follows :

Add.	Name	Bit							
		7	6	5	4	3	2	1	0
$0C	NEG_MODE	-	-	-	NEG_SPEED				NEG_PRG
$0D	LOOP_STA	-	-	-	-	STA_V22L	STA_V22A	STA_V54E	STA_V54D
$0E	HSHK_PHA	HSHK_PHA							

Where the NEG_MODE byte indicates the issue of the rate negotiation. Its meaning is :

Field	Position	Value	Description
NEG_PRG	0	0 1	Negotiation in progress Negotiation completed
NEG_SPEED	4..1	0 1 2 3 4 5 6 7 8	Reserved Reserved Negociated speed is 1200 bps Negociated speed is 2400 bps Negociated speed is 4800 bps Negociated speed is 7200 bps Negociated speed is 9600 bps Negociated speed is 12000 bps Negociated speed is 14400 bps

The LOOP_STA byte provides information about the loop status, for V.22bis and V.54 loops. This status byte must be used in accordance with the V22L2 and V54 commands. Its meaning is :

STA_LOOP		
Field	**Pos.**	**Meaning when set**
STA_V54D	0	V.54 pattern detected : when set 256 bit of the V.54 pattern has been detected
STA_V54E	1	V.54 pattern completed : when set the transmit V.54 pattern has been completely send
STA_V22A	2	V.22bis alternate "0101" or "1010" pattern detected (typicaly 53ms)
STA_V22L	3	V.22bis loop pattern detected (typicaly 13ms)
Reserved	7..4	Reserved

The HSHK_PHA byte provides information about the handshake phase state (automode, V.32bis, V.32, V.22bis, V.22, Bell 212A). This is a number between 0 and 255 that is associated with some handshake events. Refer to the "RAM mapping application note" to obtain the event equivalence table.

II.5.4 - Default Optional Status in FAX Modem Mode

While in the FAX modem mode (V.17, V.33, V.29, V.27 or V.21 channel 2) the format of the STAOP word is as follows :

Add.	**Name**	**Bit**							
		7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$0C	NEG_MODE	-	-	-	NEG_SPEED (2)				NEG_PRG (1)
$0D	STAOP1	Not used							
$0E	HSHK_PHA	PNSUCs	PRDETs	PNDETs	SCR1s	PRs	PNs	P2s	P1s

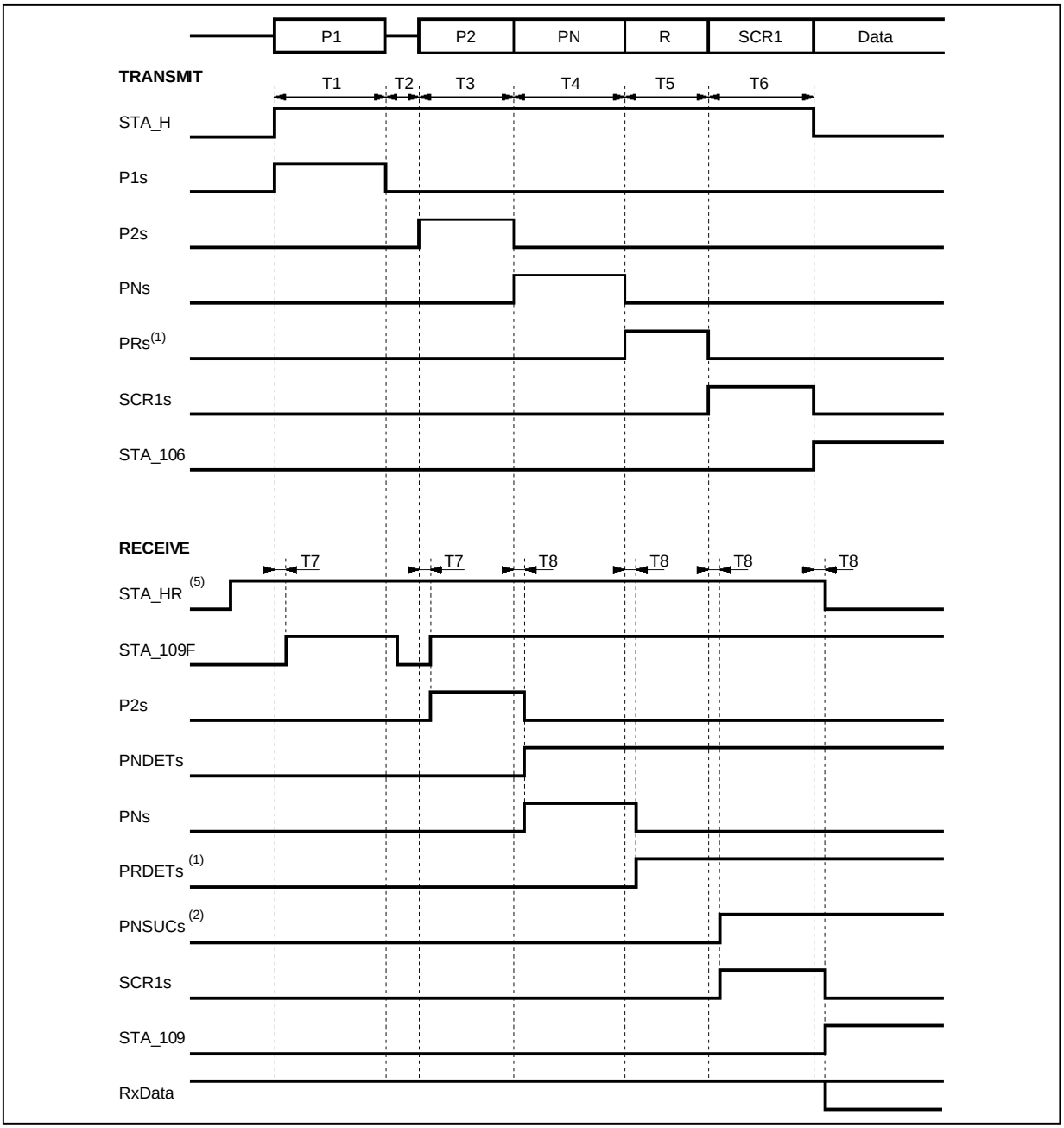
Notes : 1. SPVAL is active in V.33 receiver only at the same time as the rising transition of the SCR1s signal. Went SPVAL is set, it indicates that the SPEED bits contain the data speed information.

2. SPEED is valid in V.33 receiver only. It can have 2 values, after the SCR1s signal goes high : 1000 for 14400bps and 0111 for 12000bps.

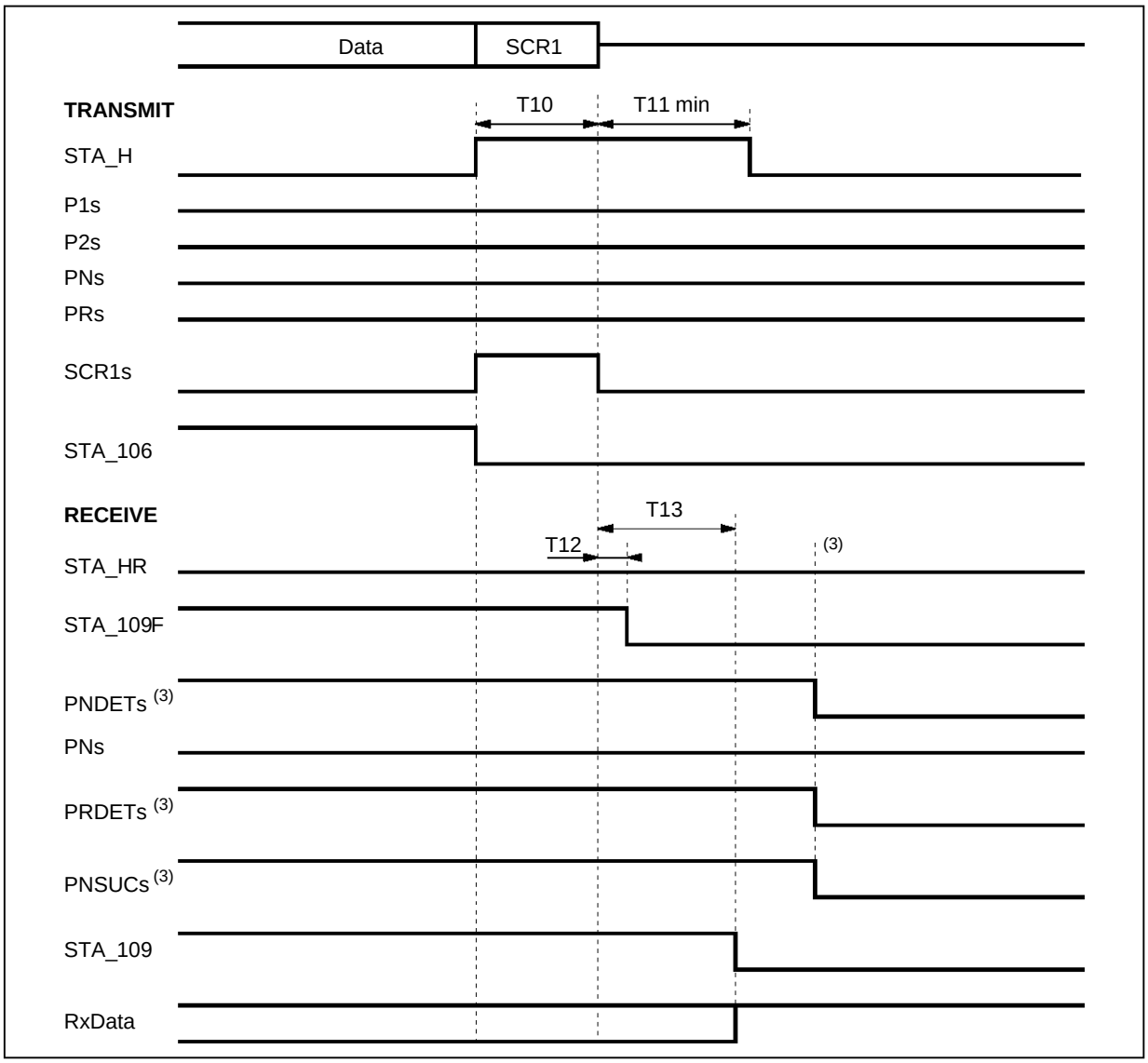
3. The HSHK_PHA bit reflects the progression of the synchronization.
It has the following meaning :

Name	**Position**	**Description**	**Tx**	**Rx**
P1s	0	Unmodulated carrier sequence. Optional, used for echo protection.	X	
P2s	1	Continuous 180° phase reversal sequence	X	X
PNs	2	Equalizer trainning sequence	X	X
PRs	3	V.33 and V.17 rate sequence	X	
SCR1s	4	Continuous scrambled 1 sequence	X	X
PNDETs	5	Turned on after PN sequence detection		X
PRDETs	6	Turned on after PR sequence detection (V.33 and V.17 only)		X
PNSUCs	7	Turned on after succesfull training of the receive equalizer. When on at the end of the synchronization, the transmition BER is statisticaly bellow 10ppm.		X

With the following timing :



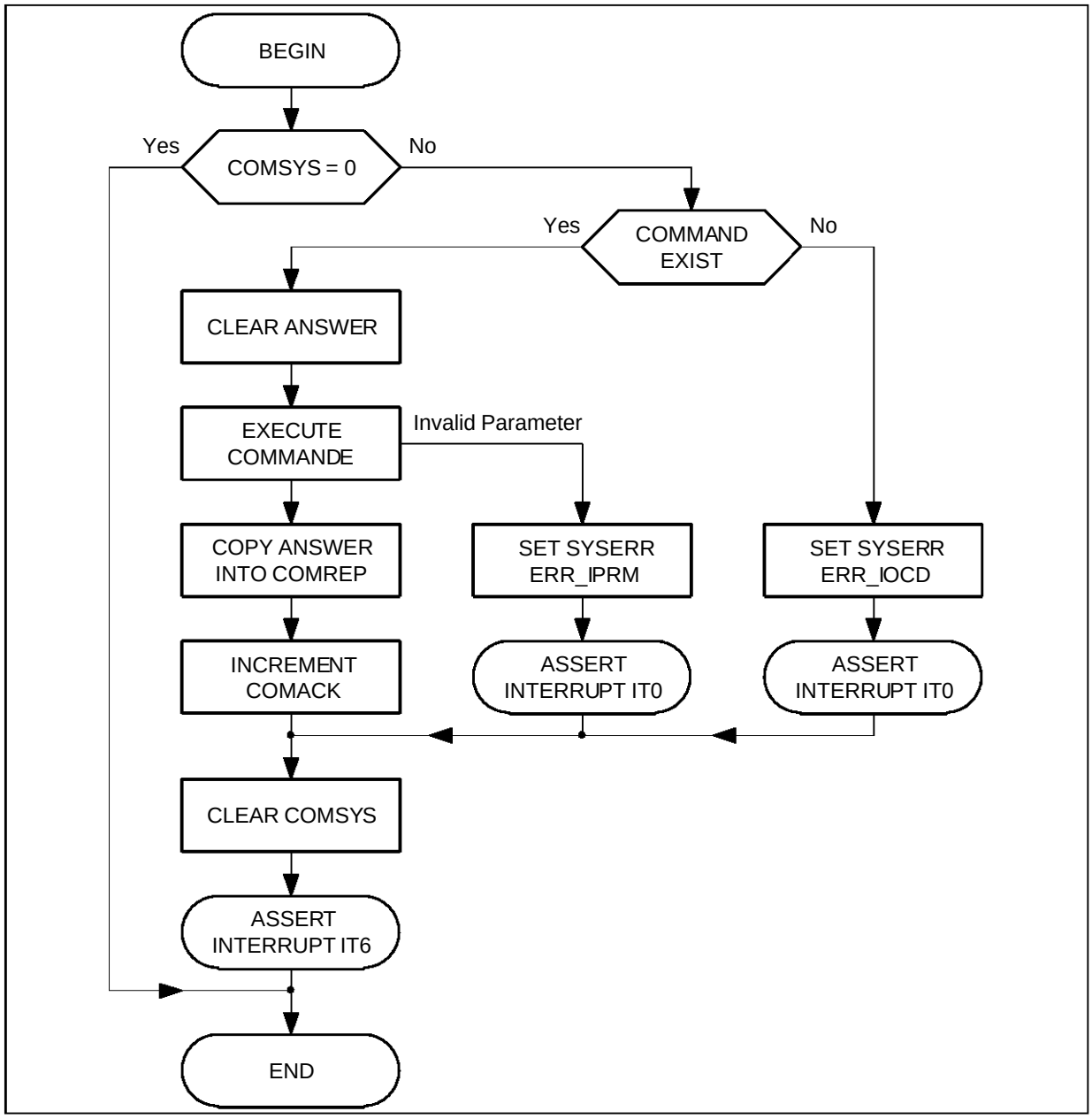
Mode	**T1** (4)	**T2**	**T3**	**T4**	**T5**	**T6**	**T7**	**T8**	**Unit**
V.17	192	22	107	1240	27	20	5	7	ms
V.17 short	192	22	107	16	0	20	5	7	ms
V.29	192	22	53	160	0	20	5	7	ms
V.29 short	192	22	41	26	0	8	5	7	ms
V.27 4800	192	22	31	670	0	5	5	7	ms
V.27 4800 short	192	22	9	36	0	5	5	7	ms
V.27 2400	192	22	42	895	0	7	6	7	ms
V.27 2400 short	192	22	12	48	0	7	6	7	ms



Mode	T10	T11	T12	T13	Unit
V.17	13	20	8	25	ms
V.17 short	13	20	8	25	ms
V.29	13	20	8	25	ms
V.29 short	13	20	8	25	ms
V.27 4800	20	30	8	25	ms
V.27 4800 short	20	30	8	25	ms
V.27 2400	27	40	8	25	ms
V.27 2400 short	27	40	8	25	ms

Notes : 1. In the case of V.29 or V.27, PRs and PRDETs bits are not active.
2. PNSUCs indicates the quality of the Rx signal that will give a ber of approximation of 10^{-5}. PNSUCs is sampled at the end of sequence PN (R for V.17). The quality is resampled and PNSUCs is recalculated 256 Bauds (106ms for V.17, V.29 ; 160ms for V.27 4800bps and 212ms for V.27 2400bps) after the falling edge of SCR1s.
3. After sending the command SYNC0, all bits are reset.
4. When using long echo protection tone, otherwise 0.
5. After sending the command SYNC1, this bit is set.

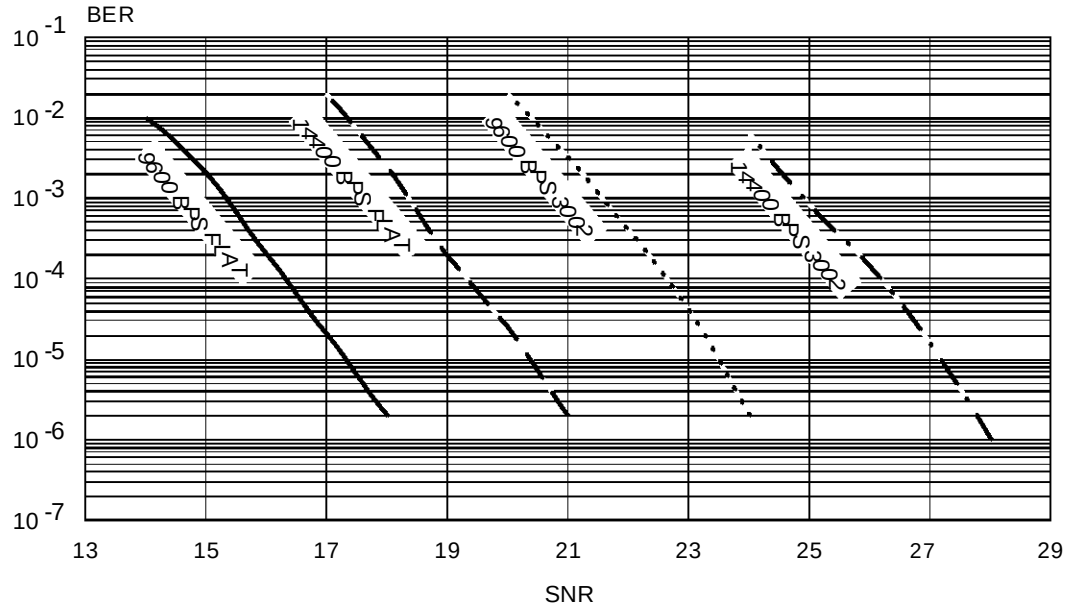
Figure B1 : Command Acknoledge



APPENDIX C : TYPICAL BER PERFORMANCES

This appendix shows the typical Bit Error Rate curves obtained on lines Flat and US3002, using a TAS® Series II equipment and a V.56 AGC. Sample size is 10^7 bit.

Figure C1 : Typical V32bis BER Performances



APPENDIX D : DEFAULT CALL PROGRESS TONE DETECTORS

Figure D1 : Call Progress Tone Detector Band 0

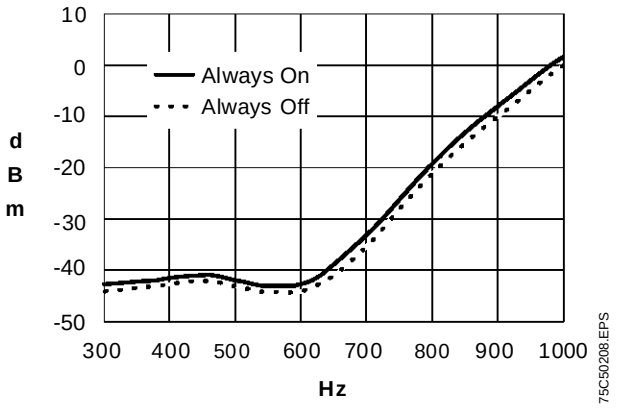
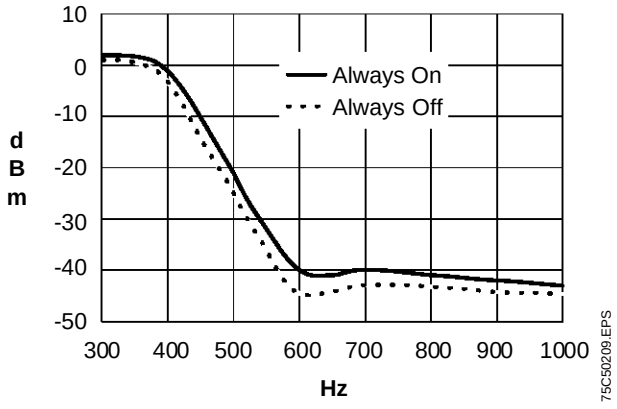
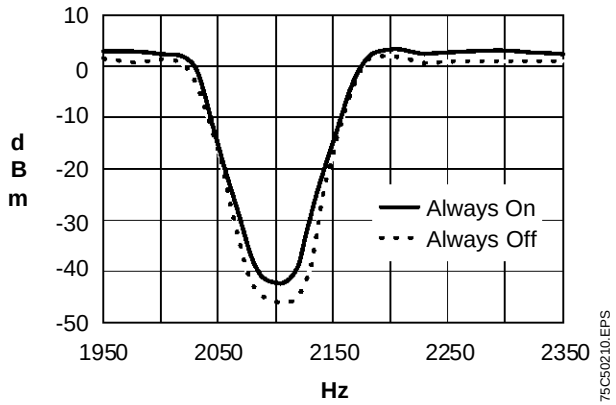


Figure D2 : Call Progress Tone Detector Band 1



APPENDIX E : DEFAULT ANSWER TONE DETECTORS

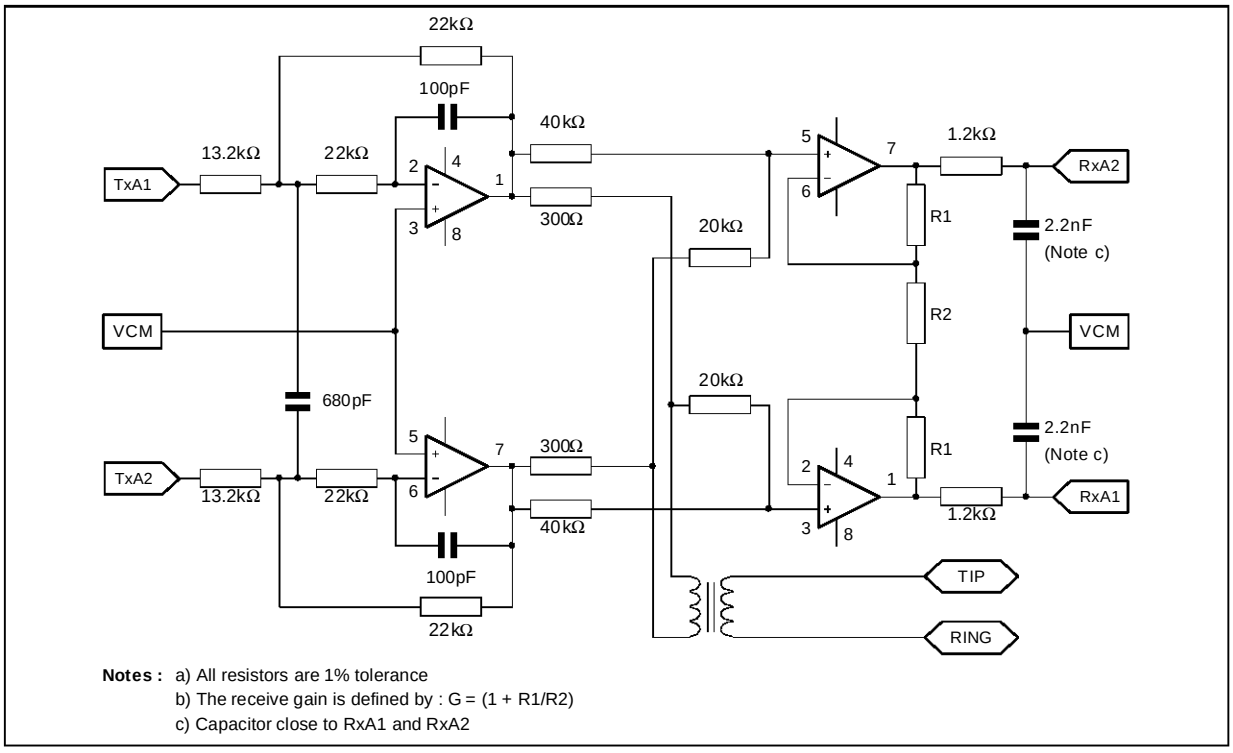
Figure E1 : 2100Hz Answer Tone Detector



APPENDIX F : ELECTRICAL SCHEMATICS

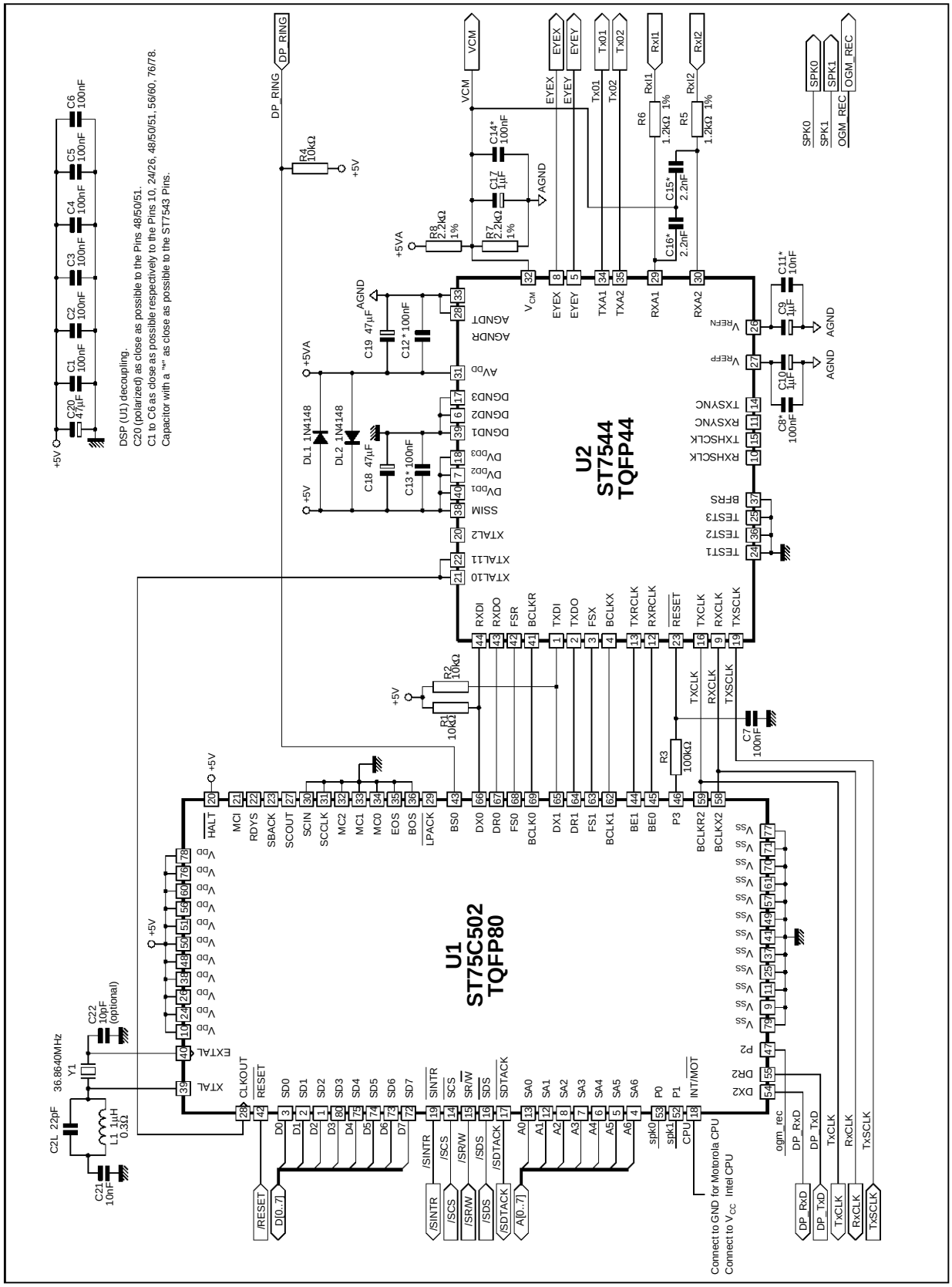
This appendix contains the following schematics :
- example of hybrid line design,
- chip interconnect circuitry required in the case of the minimal configuration.

Figure F1 : Typical Line Interface



Notes : a) All resistors are 1% tolerance
b) The receive gain is defined by : G = (1 + R1/R2)
c) Capacitor close to RxA1 and RxA2

Figure F2


DSP (U1) decoupling.
C20 (polarized) as close as possible to the Pins 48/50/51.
C1 to C6 as close as possible respectively to the Pins 10, 24/26, 48/50/51, 56/60, 76/78.
Capacitor with a "*" as close as possible to the ST7543 Pins.
U1
ST75C502
TQFP80
U2
ST7544
TQFP44
Connect to GND for Motorola CPU
Connect to VCC Intel CPU
75C50222.EPS

APPENDIX G

I - TONE DETECTORS

I.1 - Overview

The general purpose TS75C50/51/52 tone detector block is a powerful module that covers a lot of applications :

- call progress tone detection, fully programmable for all different countries,
- DTMF detection,
- high level handshake for all main modem standards,
- FAX, voice, data automatic detection,
- call waiting detection, while in voice or data mode.

I.2 - Description

The tone detector block is a set of 16 identical cells. Each cell is composed of a double biquadratic filter, a power estimator section, a static level and a level comparator.

Each biquadratic filter, power estimator and static level can be programmed using a complete set of commands (TDRC, TDRW, TDWC, TDWW, TDZ).

The wiring between the different cells can be defined by the user using the command allowing a wide range of applications.

The 16 comparator outputs give, on a baud basis, the information into a two 8 bits word TONEDET0 (for cells number 0 to 7) and TONEDET1 (for cells number 8 to F). These TONEDET variables can be accessed using a MR command or, more easily, monitored on a baud basis using the DOSR command.

While in FAX half duplex receive IDLE mode a set of 8 cells allows to implement customized handshake short sequences.

I.2.1 - Biquadratic Filters (see Figure G1)

Each biquadratic filter is a double regular section that can perform any transfer function with 4 poles and 4 zeros. This routine is run on a sample basis.

The corresponding transfer function is :

$$\frac{Out}{Input} = C0 \cdot \frac{C5 + 2 \cdot C3 \cdot z^{\pm 1} + 2 \cdot C4 \cdot z^{\pm 2}}{1 \pm 2 \cdot C1 \cdot z^{\pm 1} \pm 2 \cdot C2 \cdot z^{\pm 2}} \cdot C6 \cdot \frac{CB + 2 \cdot C9 \cdot z^{\pm 1} + 2 \cdot CA \cdot z^{\pm 2}}{1 \pm 2 \cdot C7 \cdot z^{\pm 1} \pm 2 \cdot C8 \cdot z^{\pm 2}} \cdot z^{\pm 1}$$

Note : All coefficients are coded on 16 bits 2's complement in the range +1, -1 (Q15). To avoid the possibility of overflow the user must check that the internal node must not be higher that 0.5 (in Q15 representation).

I.2.2 - Power Estimation (see Figure G2)

The power estimation cell is needed to measure the amplitude of the different tones. It is run on a sample basis.

The corresponding transfer function is :

$$Out = |\ Input\ | \cdot z^{-1} \cdot \frac{P1}{1 \pm (1 \pm P1) \cdot z^{\pm 1}}$$

Note : To deal with the high dynamic range of the analog front end, the computation loop of the power estimation is run with 32 bits accuracy. The output and input of that cell are however 16 bit words (Q15).

Figure G1 : Biquadratic IIR Filter

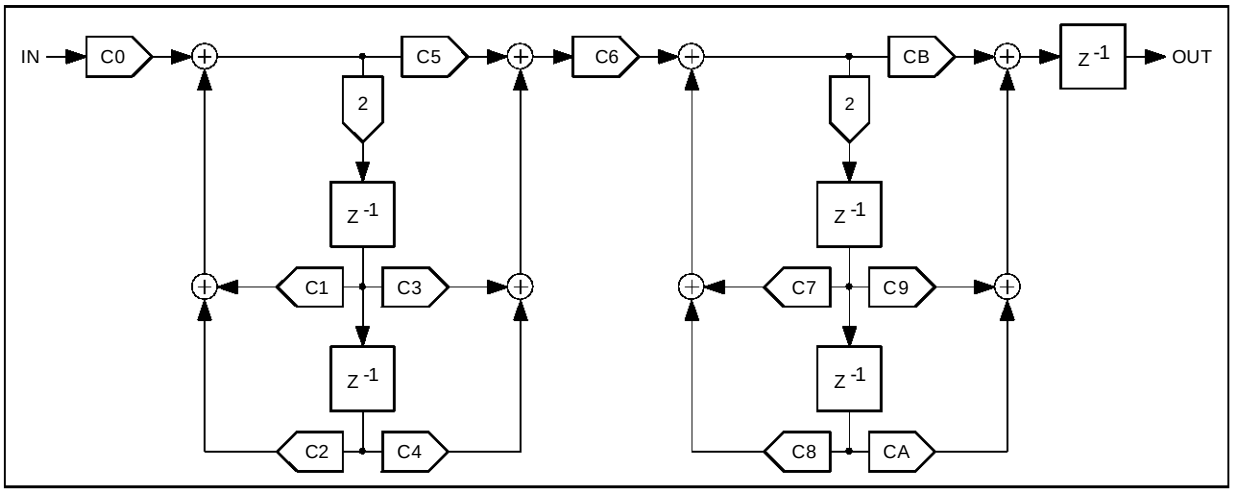
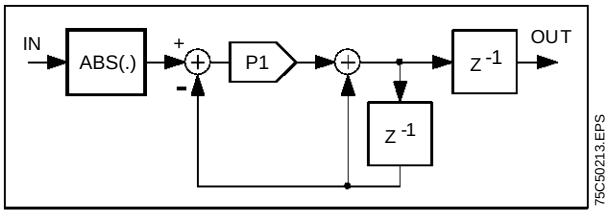


Figure G2 : Power Estimator



I.2.3 - Static Level

A single threshold level is associated with each cell. It can be use to compare the output of a power estimation with an absolute value.

I.2.4 - Comparator

The comparator computes on a baud basis, the difference of the signal on its positive input and its negative input. If the result is higher that zero it set the corresponding bit in the TONEDET[0..1] word if not it clears this bit.

I.2.5 - Wiring

The user must specify the connection (wiring) between the input/output of the filter, the input/output of the power estimator, the output of the static levels and the two inputs of the comparators.

The outputs signal have an absolute address :

Node Address		
Signal Name	**Address**	**Description**
Ground	00	Signal always equal to 0000
RxSig	01	Receive signal from the analog front end, (after echo-substraction in V.32 mode)
RxSig2	02	Receive signal multiplied by 2
RxSig4	03	Receive signal multiplied by 4
	04..0F	Reserved
Filter [0..F]	10..1F	Biquadratic filter outputs
Power [0..F]	20..2F	Power estimator outputs
Level [0..F]	30..3F	Static levels

The user specifies the inputs of the filters, power and comparators. At least one input must come from the RxSig (node 01, 02 or 03). It is mandatory to connect all unused cell input to the ground signal (node 00).

III - EXAMPLE (see Figure G5)

Hereunder is an example of programming a single tone detector (using cell #3) and a complex differential tone detector (using cell #4 and #5).

The bit 3 of the TONEDET variable will be triggered each time the energy of that filtered signal is higher than static level number 3.

The bit 4 of the TONEDET variable will be on each time a receive signal has energy higher than the static level number 4. The bit 5 will be on only when the filtered (filter section 4 and 5) received signal is higher than the energy of the wideband signal number 4 ; this prevents triggering on noise.

Program cell #3 :

TDWW 03 00 13 01
Connect received signal to filter and filter to energy
TDWW 03 01 33 23
Connect level to comparator negative input and energy to positive input

Program cell #4 and #5 :

TDWW 04 00 01 01
Connect received signal to filter and energy
TDWW 04 01 34 24
Connect level to comparator negative input and energy to positive input
TDWW 05 00 15 14
Connect filter #4 output to filter and filter to energy
TDWW 05 01 24 25
Connect wideband energy to negative input and energy to positive input

Figure G3 : Tone Detector Wiring Address (first half)

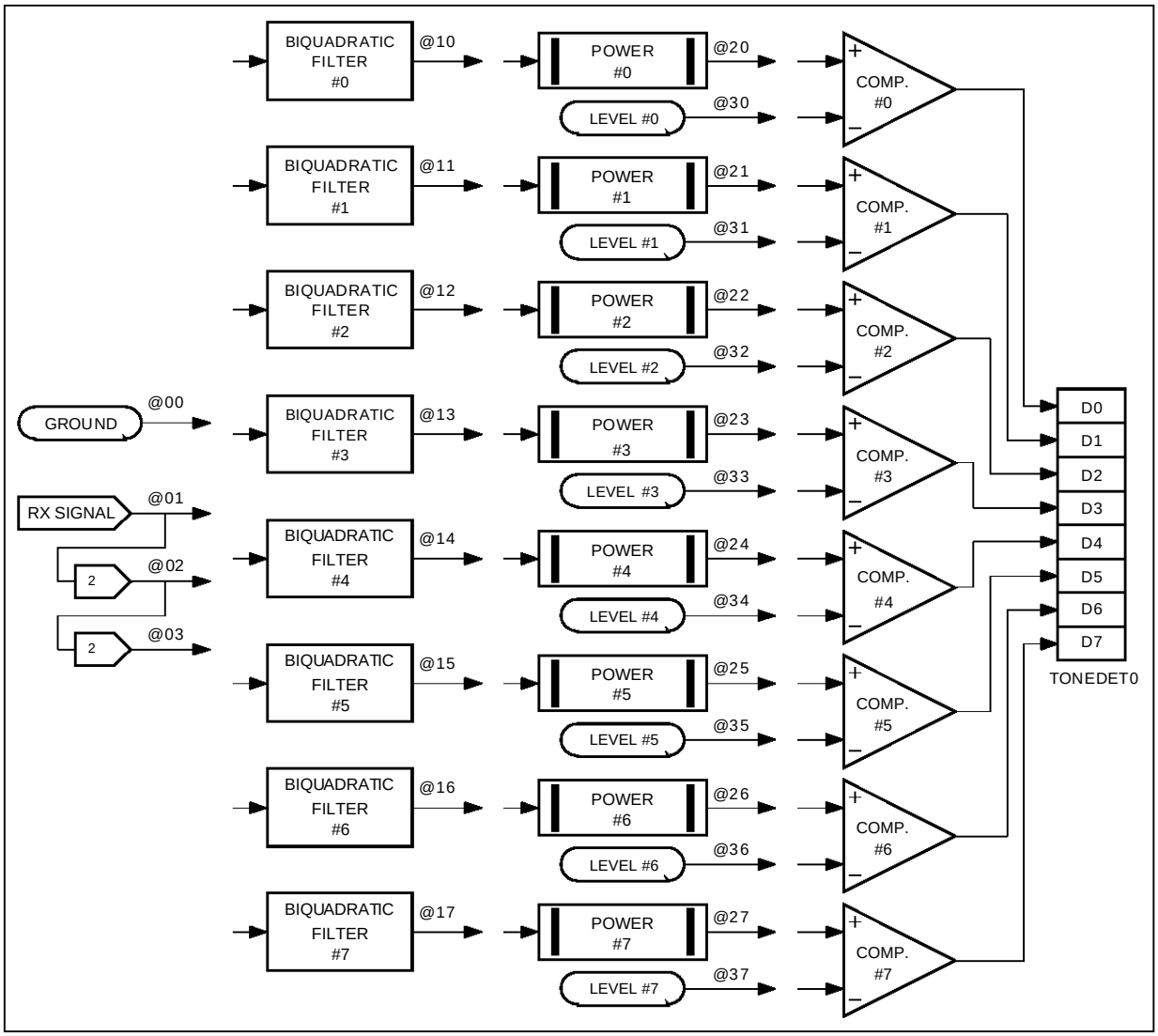


Figure G4 : Tone Detector Wiring Address (second half)

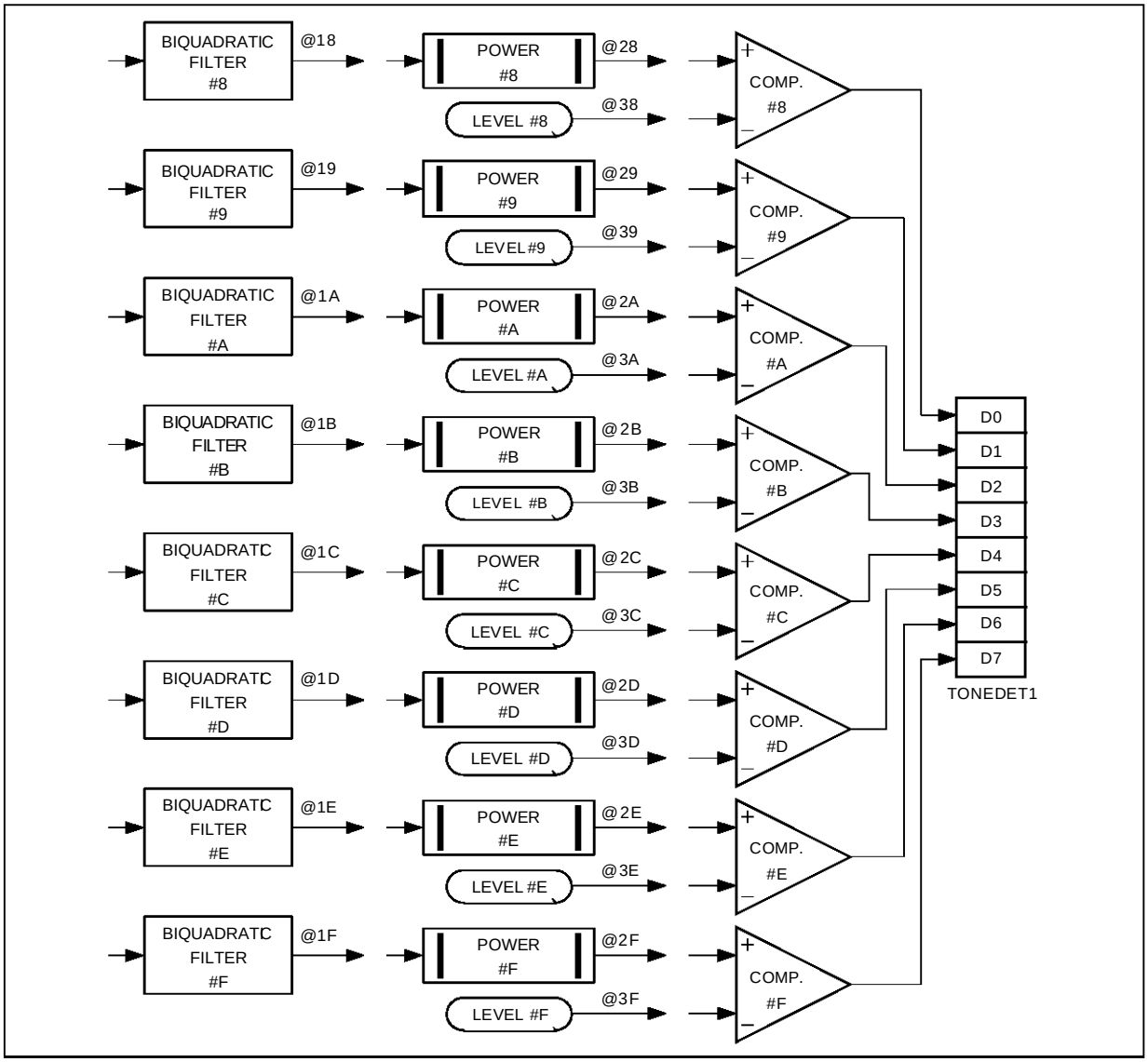
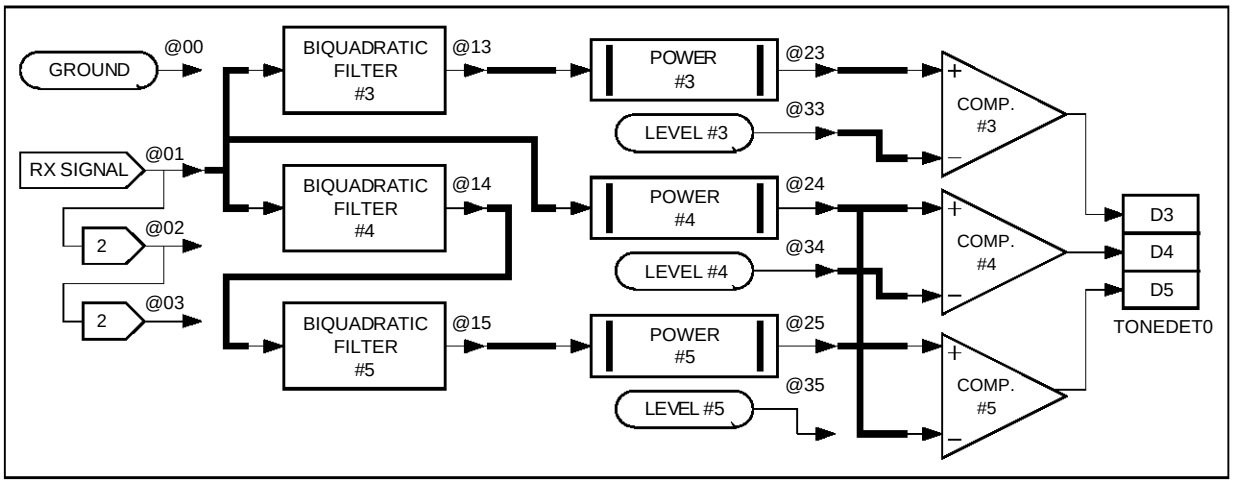


Figure G5 : Wiring Example



APPENDIX H : BUFFER OPERATIONS

I - INTRODUCTION

This appendix is dedicated to the buffer operations, either the data buffers, used either in data exchanges or the symbol buffer operations dedicated to bulk delay management.

II - RECEIVE OPERATIONS OVERVIEW

Figure H1 describes the receive data flow.
The ST75C502 uses parallel synchronous data.
8 bit words are synchronously available in the receive buffers. The buffer status holds the numbers of valid bytes received.
Each time the receiver has filled up a new buffer, it sets the corresponding flag with the proper status then generates the IT3 interrupt. The availability of the buffers is tested just before starting to fill them. This means that the host must not perform any buffer operation on the data part while the status remains 0.

III - TRANSMIT OPERATIONS OVERVIEW

Figure H2 describes the transmit data flow.
The ST75C502 uses parallel synchronous data.
8 bit words are synchronously read from the transmit buffers. The transmit status buffer holds the number of valid bytes to be transmitted (up to 8 per buffer).
Each time the transmitter has emptied a buffer, the IT2 interrupt is raised.

IV - BUFFER STATUS AND FORMAT DESCRIPTION

The following section describes the meaning and use of the buffer status words.

IV.1 - Transmit buffer

The transmit buffer status words are DTTBS0 and DTTBS1 (see the *Host Interface Summary* section in the main document) and are more likely to be seen as control words. These flags must be set by the host and are reset by the ST75C502. The data buffer exchanges being synchronized through these status words, an improper setting will trigger the error Err_Tx in the error status SYSERR. A value of 0 for DTTBS0 or DTTBS1 means that the corresponding buffers are empty : this value is written by the ST75C502. The unused bits of DTTBSx must be set to 0 by the host.

Field	Pos.	Val.	Description
BUFF_LENG	3..0	8..1	Number of valid bytes in the buffer

IV.2 - Receive buffer

The receive buffer status words are DTRBS0 and DTRBS1 (see the *Host Interface Summary* section in the main document). These flags are set by the ST75C502 and must be reset by the host. The data buffer exchanges being synchronized through these status words, an improper resetting will trigger the error Err_Rx in the error status SYSERR. A value of 0 for DTRBS0 or DTRBS1 means that the corresponding buffers are empty : this value must be written by the host.

Field	Pos.	Val.	Description
BUFF_LENG	3..0	8..1	Number of valid bytes in the buffer

Figure H1 : Rx Buffer Schematics

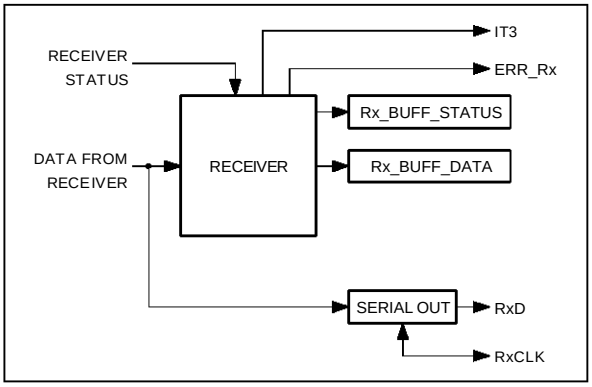
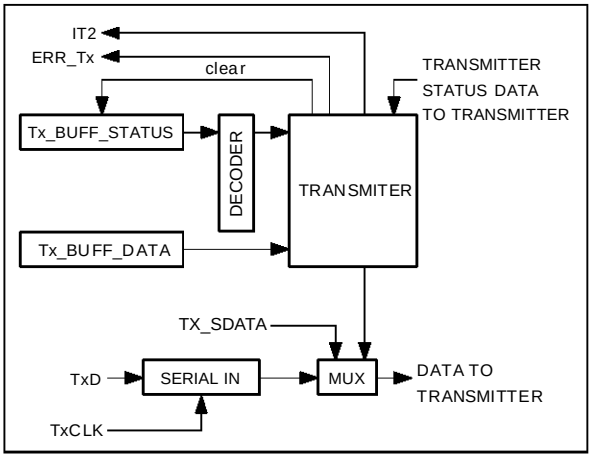


Figure H2 : Tx Buffer Schematics



V - DATA BUFFER MANAGEMENT

In the transmit path, the data buffer exchanges should always begin with the filling of buffer 0, then with the update of the buffer 0 status word. The initiation of the data exchanges is initiated then with the XMIT command.

VI - BULK DELAY MANAGEMENT

The processing of the bulk delay uses a simplified buffer exchange scheme. Each time the ST75C502 has internally buffered enough symbols, it writes them inside the symbol buffer area, then computes the address inside the host space where these symbols should be written. This address is a relative address inside the host data space, allowing thus the host to dispose this area the most convenient way. The target address is located in the SYMADR[0..1] registers under a 16-bit form.

These addresses must be defined by the user using the BULK command. It can be any valid 16 bit number assuming the base address (BA_ADDR) is on a 8 byte boudary and the top address (TO_ADDR) is higher and on a 8 byte boundary minus 1.

Eg : if we want to be able to cancel a 2 satellites Round trip delay we must have a bulk delay bigger than 2 times 560ms, lets say 1.5 seconds. The symbols needed are 1.5 · 2400 (3600 bytes). If we say that the base address is, for example, 0x4230 the top address must be 0x503F (= 0x4230 + 3600 - 1).

According to the current round trip delay, the ST75C502 computes the address of the symbols required for the far end echo computation. This address is computed (as the previous one) according to a circular addressing scheme inside the base .. top address space.

The symbol buffer status SYSSTA is then set to FF and the IT1 interrupt is raised. The host should then perform the following operations in sequence :

1) read the address SYMADR[0..1] of the target location for the symbols,
2) read SYMBU[7..0], the corresponding symbols, and store them at the addressed lolcation (8 symbols),
3) read the address SYMADT[0..1] of the symbols required by the ST75C502,
4) fetch the required 8 symbols and store them in the SYMBUF[7..0] array,
5) write the proper status word (00) in SYMSTA.

The ST75C502 meanwhile pools for the status word to be 00, then stores the symbols inside its own memory space for processing and sets the status word to its idle value FF.

VI.1 - Status Word

The status word SYSSTA can have the following values :

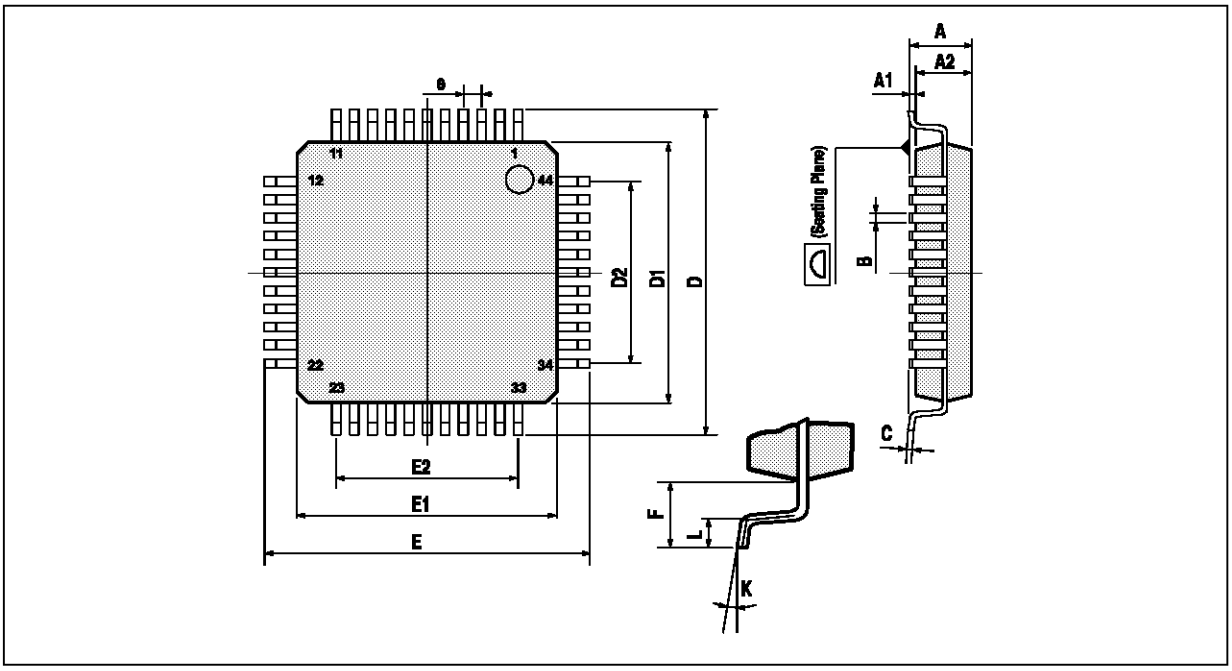
Field	Pos.	Val.	Description
SYSTA	7..0	00	Symbol buffer owned by the DSP
		FF	Symbol buffer owned by the host

VI.2 - Interrupt

Each time a symbol buffer is processed by the ST75C502 an IT1 interrupt is generated. The host has an 8 symbols time (3.3ms) to process this interrupt otherwise an error occurs that will be signaled into the SYSERR bit 2 ERR_SYM.

PACKAGE MECHANICAL DATA

44 PINS - PLASTIC QUAD FLAT PACK (THIN)

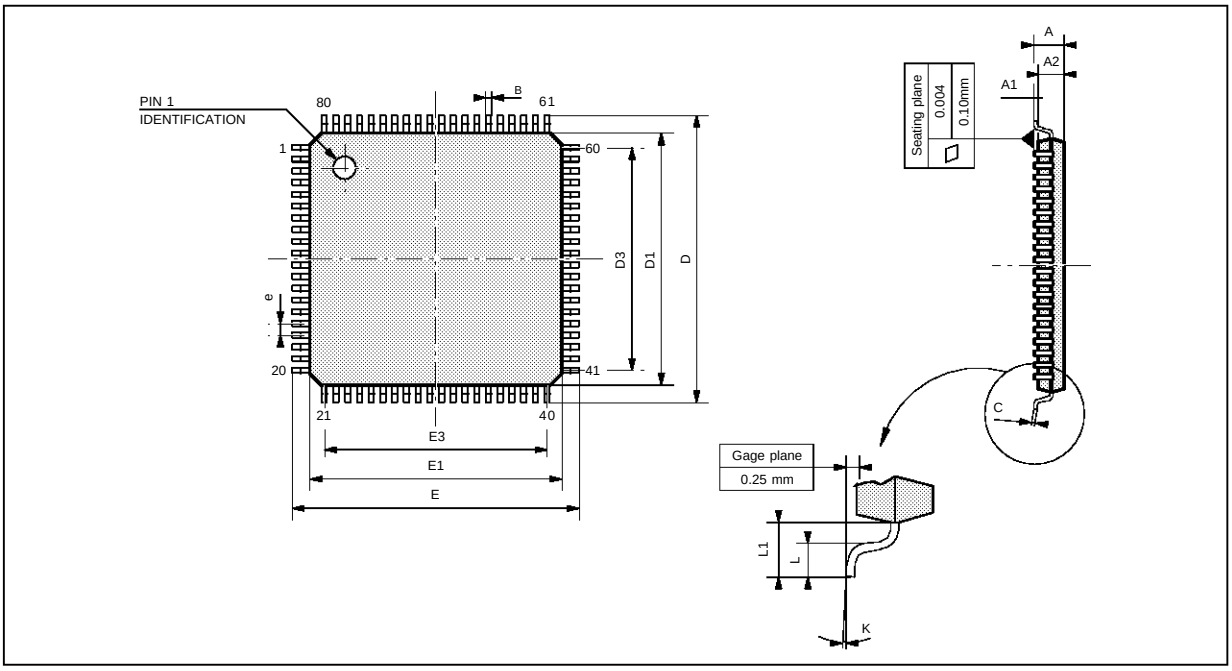


PMPQFP44.WMF

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1		0.25			0.01	
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.35		0.50	0.014		0.020
C			0.17			0.007
D	15.75	16.00	16.25	0.620	0.630	0.640
D1	13.90	14.00	14.10	0.547	0.551	0.555
D2		10.00			0.394	
e		1.00			0.039	
E	15.75	16.00	16.25	0.620	0.630	0.640
E1	13.90	14.00	14.10	0.547	0.551	0.555
E2		10.00			0.394	
F		1.60			0.063	
K	0^o (min.), 7^o (max.)					
L	0.45	0.60	0.75	0.018	0.024	0.030

TQFP44.TBL

PACKAGE MECHANICAL DATA (continued)
80 PINS - PLASTIC QUAD FLAT PACK (THIN)



PMTQFP80.EPS

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.22	0.32	0.38	0.010	0.012	0.014
C	0.09		0.20	0.004		0.008
D		16.00			0.630	
D1		14.00			0.551	
D3		12.35			0.486	
e		0.65			0.0314	
E		16.00			0.630	
E1		14.00			0.551	
E3		12.35			0.486	
L	0.45	0.60	0.75	0.020	0.024	0.030
L1		1.00			0.039	
K	0^o (min.), 7^o (max.)					

TQFP80.TBL